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REVISION 1

FINAL REPORT - PHASE I

NON-DESTRUCTIVE READOUT DATA MEMORY UNIT

JPL Contract No. 950986

Prepared for:

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California Institute of Technology
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ABSTRACT

This document reports the technical results of Phase I of a multiphase program for the development of a small, low-power, nondestructive-readout data memory unit for space application. The prototype and the ultimate flight memory systems will store 1024 words each of 20 binary digits using the advanced woven plated wire memory element and integrated circuits.

In general summary, the Phase I effort comprised the design, fabrication, test and evaluation of a breadboard system containing a memory stack fabricated to package design and construction standards essentially identical to those for the prototype to be fabricated in Phase II. The breadboard system stores 256 words of 16 binary digits each. Its purpose is twofold: to demonstrate circuit electrical performance and the environmental and electrical performance and characteristics of the encapsulated memory stack for application in the prototype memory system. In addition, the Phase I effort included a study and formulation of the packaging for the prototype system, and the design and fabrication of a nondeliverable memory exerciser, capable of interfacing with either the breadboard or prototype system at the prescribed signal levels.

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Section 1

INTRODUCTION

1.1 PURPOSE OF THIS REPORT

This document reports the technical results of Phase I of a multiphase program for the development of a small, low-power, nondestructive-readout data memory unit for space application. The prototype and the ultimate flight memory systems will store 1024 words each of 20 binary digits using the advanced woven plated wire memory element and integrated circuits.

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One of the two encapsulated memory stacks fabricated in Phase I was tested over a wide range of temperature, shock, vibration, and sterilization environments and, with minor exceptions, successfully passed all tests. The breadboard system successfully passed its acceptance tests without exception.

The characteristics of the breadboard and prototype memory systems are summarized in Section 1.2. Section 2 describes the woven plated wire memory planes around which the memory system is designed. The electrical design of both breadboard and prototype memory systems is described in Section 3, which constitutes the main body of this report.

Section 4 covers packaging design and fabrication of the breadboard system. Section 5 reports the results of the Packaging Study for the Phase II prototype memory. Section 6 reports the procedures for and results of the evaluation of Phase I hardware and Section 7 contains a suggested Statement of Work for Phase II.

1.2 SUMMARY DESCRIPTION OF THE MEMORY

This section presents the salient features of the prototype and flight memory systems; data for the breadboard system, which electrically is a scaled-down version of the prototype, are shown in parentheses where they differ from those of the prototype.

Capacity: 1024 words of 20 binary digits each, a total of 20,480 bits (the breadboard has 256 words of 16 bits, total 4096 bits).

Storage Means: Magnetic, on a thin film of permalloy plated on a copper alloy wire substrate.

Electronics: All solid state, all silicon. No moving parts.

Volatility: Nonvolatile. Stored information is retained in the absence of power and can be read out as soon as power is restored.

Data Transfer Mode: Bit serial. One input wire for writing, one output wire for reading.

Addressing: Random by word. External equipment supplies ten (eight for the breadboard) bits of word address. Serial by bit within the word. A CLEAR signal, when used, resets the memory bit counter to bit 1 of the 20-bit word.

Data Transfer Rate: 0 to 100,000 bits per second, as paced by a clock signal supplied to the memory from external equipment.

Signal Interface: Compatible with all common TTL and DTL logic systems.

Readout Mode: Nondestructive. Reading data from the elementary magnetic storage cells leave the states of their magnetization unaltered; no "restore" cycle is needed.

Data Alteration: New Information can be entered into the memory at any time, at any data rate up to 100,000 bits per second. New data is written over the old, no "erase" operation is required.

Marker Outputs: Five selected bits of the 20 in a word may be connected to bit marker output lines which give an indication when the memory operates on the bit so marked.

Power Consumption: 40 mw on standby. An increment proportional to data transfer rate is added when the memory is used. At maximum data rate, power consumption is 230 mw for READ, 240 for WRITE.

Power Supply Requirements: +15 VDC, +5 VDC, and -3 VDC, all ±10 percent.

Size: 5 x 6 x 1.6 inches; volume 48 cubic inches (prototype only).

Weight: Four pounds (prototype only).

Ambient Temperature: -10°C to +85°C.

Shock: To 10,000 g's, any direction (prototype only).

Vibration: (prototype only)

1 to 4.4 Hz:	±1.5 inches displacement
4.4 to 15 Hz:	±3.0g peak acceleration
15 to 40 Hz:	5.0g rms white noise (15-2000 Hz) plus
	2.0g rms sinusoid, applied simultaneously
40 Hz to 2000 Hz:	5.0g rms white noise (15-2000 Hz) plus
	9.0g rms sinusoid, applied simultaneously

Humidity: 0 to 75% at 38°C.

Altitude: No restrictions.

1.3 PROGRAM HISTORY

The present program originated with the planning of electronic component and systems requirements for future NASA space missions by the Jet Propulsion Laboratory of the California Institute of Technology. Because the memory is the most critical element in most digital systems, it was one of the first system components of a new family to be defined and placed under development by JPL. Specifications for the memory were designed to permit its application in as broad a spectrum of programs as possible.

JPL solicited proposals for the new memory unit from several carefully-selected bidders early in July 1965; proposals were submitted seven weeks later. After a period of negotiation, General Precision was awarded a two-phase contract dated April 1, 1966 for development of the memory.

The breadboard memory unit designed, fabricated, and tested under Phase I of this contract successfully passed acceptance testing on December 10, 1966. This report will complete Phase I requirements.

Under Phase II of the contract, a prototype memory, designed to be capable of meeting flight hardware requirements, will be fabricated and tested. This phase will be completed before the end of 1967.

1.4 CONFORMITY TO JPL DESIGN GUIDELINES

The Design Guidelines of Exhibit I to the Contract are here reviewed with reference to the memory design produced during Phase I of the program.

Power Consumption

(Quoting from Exhibit I) "Power is a major constraint in spacecraft. The specified power consumption is the maximum that can be allowed..."

The original RFP specified power maxima of 10 watts operating and 1 watt standby. The General Precision proposal showed calculated maxima of 275 mw and 43 mw, respectively; contract figures were set at 500 and 100 mw. New calculations based on designs completed in Phase I put power dissipation of the prototype memory at 240 mw writing, 230 mw reading, both at 100 kHz, and at 40 mw standby. The breadboard should be the same on standby and about 6 mw less operating; actual measurements on the breadboard were 270 mw writing, 240 mw reading, and 32 mw standby. No attempt has been made to minimize breadboard power dissipation by reducing pulse widths in the timing circuitry; variations from nominal widths are responsible for the discrepancy in operating power. Standby dissipation is less than calculated because the particular read preamplifier installed in the system, an integrated circuit, draws less than the nominal current specified by the manufacturer.

Minimum Semiconductor Count

"The electronic components which generally seem to have the highest failure rates are semiconductor elements ... Minimizing the number of these elements is, therefore, of considerable importance."

The original proposed system configuration, which has been followed in Phase I, minimized component count by using a single read amplifier and digit driver for access to all storage locations, a possibility suggested by the low data rate and the development of an advanced type of woven plated wire memory plane.

Proposed and current circuit designs (which differ only slightly) minimize semiconductor count through maximum use of monolithic integrated circuits and through frequent use of highly-efficient transformer coupling. The prototype memory will have 18 integrated circuits, 155 discrete transistors, 295 discrete diodes plus 256 pairs of redundant diodes in the stack, based on current designs.

Component Derating

"Component failure rates are generally related to various electrical stress values: power dissipation, junction voltages, etc. Operating all components significantly below their maximum ratings should greatly enhance the reliability of the system."

Because of the low power, voltage, and current levels at which the memory system operates, it has generally been very easy to design circuits in which worst case stresses on components are much lower than manufacturers' ratings. However, reverse transistor emitter diode voltage ratings for a few sockets have been a problem to which a final solution was not reached in Phase I. See Section 3.4 for further details.

Use of Analog Type Circuits

"Circuits which place stringent requirements on component parameter tolerances, such as sense amplifiers, are to be avoided as far as possible." It has proven to be possible to avoid all but one sense amplifier. Most of the required amplification of the sense signal from the stack is achieved

with a single monolithic integrated circuit, the Fairchild 702A operational amplifier. Some additional amplification is obtained with discrete components. Strobing in the Read Amplifier Shaping Network changes the read signal to digital form.

Digit and word current amplitude specifications for the array require current regulators (the Digit Current Sink and the Word Pulse Generator). A voltage regulator is used to supply power to most of the addressing circuits. In all three cases, selected trimming resistors, rather than potentiometers, will be permanently installed during fabrication to set initial current and voltage values. All circuits can tolerate aging drifts up to several percent, and there should be no problem in achieving this stability through use of metal film resistors; the effects of transistor parameter drifts have been largely eliminated through use of heavy negative feedback.

Analytical Circuit Designs

"The required formal documentation regarding circuit design is being limited to schematics and specifications ... Any future flight hardware which might evolve from this development would require complete documented analytical design of all circuits used."

Circuit designs are based on calculations using worst case combinations of imposed conditions, component parameter values, and aging drift. However, a few difficult problems have been left for Phase II. See Section 3.4.2. Worst case analyses are not formally documented in this report.

Use of Integrated Circuits

"Integrated circuits shall be used where applicable to the system. The use of integrated low level logic modules and integrated sense amplifiers shall be a design objective ..."

An integrated circuit, the Fairchild 702A, is used for the read preamplifier; sixteen Signetics SE455J dual TTL gates are used in the prototype word electronics, and a Signetics CS720J quad two-input DTL gate is used for the digit driver and read/write control circuits. The input stages of the D switch are presently shown as discrete DTL gates; they will very

likely be changed to monolithic integrated circuit gates in Phase II. Additional monolithic integrated circuit gates will be included in the prototype as input buffers if customer specifications are changed to require compatibility with Fairchild 9000 Series Low Power DTL logic; they will not replace any existing circuitry.

The proposed use of hybrid integrated circuits has been abandoned in favor of cordwood circuit modules using discrete components.

Interconnections

"... to minimize the probability of a failure ... (A) Minimize the number of interconnections (B) Use a controllable, reproducible process for making interconnections, such as welding."

The use of monolithic integrated circuits has reduced the number of connections, and placing the diode word matrix in the memory stack has reduced the number of wires leaving the stack. But the total number of connections in the prototype system has grown considerably during Phase I because of the decisions not to use hybrid integrated circuits and to place more emphasis on repairability.

Present plans for the prototype call for circuit modules to be soldered, with each solder joint to be given the same degree of careful planning and control as is customarily done for welding.

Components

"A memory system using state-of-the-art technology is desired ... components which do not appear able to withstand sterilization or are inherently fragile shall not be used ... All components used in any flight hardware evolving from this development must be qualified for inclusion in the JPL-preferred parts list or qualified to an equivalent level."

Integrated circuits have been used in the design wherever possible, as discussed above. The most advanced element used in the memory is the woven plated wire memory plane itself. This component was not suitable for severe shock and vibration environments in the package forms in which it was commercially available at the start of this program, and a major

effort to develop fabrication techniques and packaging designs suitable for this and other aerospace applications was undertaken by Librascope early in 1966. Two encapsulated memory stacks were then fabricated as part of this program; one was tested in wide range temperature, shock, vibration, and sterilization environments to evaluate the new packaging designs; no major problems in meeting space requirements have been revealed by these tests.

All other components are conventional, although the particular sizes and styles specified are frequently of recent design. The memory has no moving parts.

Packaging Techniques and Materials

"It is expected that a memory system which is sterilizable and capable of withstanding an extremely high impact environment will evolve from this development. A modularized system is desired for maintainability and a minimum number of interconnections is desired for maximum reliability..."

A prototype packaging study was performed as part of Phase I of the program; results are presented in Section 5. The present package design, developed in close liaison with JPL engineers, is extremely rugged, yet small and repairable. It consists essentially of two electronic assemblies with a total of 54 compact cordwood circuit modules, one on each side of an encapsulated memory stack. A rugged aluminum housing which conforms to JPL subchassis form standards encloses the stack-electronics sandwich. Volume is 48 cubic inches.

1.5 REFERENCES

Significant documents pertaining to the present effort are:

JPL Statement of Work No. 7246, dated June 11, 1965

JPL Exhibit I to the Statement of Work, dated June 11, 1965

JPL Request for Proposal No. 7246, for Development of Nondestructive Readout Data Memory Unit, July 6, 1965.

General Precision-Librascope Proposal No. EX5-1047-BI, Nondestructive Readout Data Memory Unit, dated August 27, 1965

General Precision-Librascope Addendum No. EX5-1047-BI, Revised Work Statement, dated October 21, 1965

JPL Contract No. 950986, Nondestructive Readout Data Memory Unit, dated April 1, 1966

JPL Contract No. 950986, Modification No. 1, Supplemental Agreement, dated November 3, 1966

Section 2

WOVEN PLATED WIRE MEMORY PLANES

The memory device used in the low-power space memory system is of woven plated wire. The particular memory plane configuration used in the breadboard has two woven memory mats; one mounted on each side of an epoxy glass board. Memory mats are nondestructive read types designated MX-W32D64(80)-2VNN. A complete plane has a capacity of 4096 data bits arranged in a 64 x 64 aspect ratio. The plane is encapsulated in a silicone rubber compound. Details of plane performance and structure are provided in Section 2.4. Woven plated wire memory operating and fabrication processes are reviewed in Section 2.1 through 2.3.

The storage elements in the woven plated-wire memory planes are lengths of wire upon which a magnetic material has been electroplated to produce a cylindrical magnetic thin film. The magnetic electroplate is deposited in the presence of a circumferentially oriented magnetic field, which imparts a circumferential uniaxial magnetic anisotropy to the film. A memory matrix is fabricated by weaving plated wires as the woof and insulated wires as the warp. Fine wires are used to produce high-density weaves.

The memory bit in its simplest form is shown in the shaded circle of figure 2.0-1.

The plated wire serves as a combination digit and sense line, as well as the storage medium. Magnetization by digit current is in the "easy" (circumferential) direction. Segments along the plated wire are enclosed by word windings formed of the insulated wire warp. Current along word windings generates a "hard" (axial) direction magnetic field in the plating. Data is stored in the rings of magnetic film at digit and word line intersections. Although the plating on the wire is continuous, only sections in close proximity to the word windings contribute to memory operation. Thus, a single plated wire is electrically divided into many memory

elements. Interaction between bits is made negligible by suitable plating processes, field shaping, and spacing of word lines.

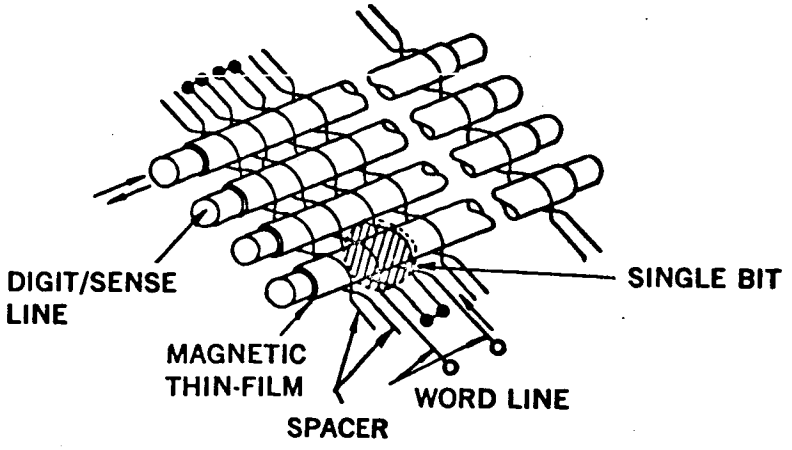


Figure 2.0-1. Location of a Stored Bit

A particular advantage of weaving plated-wire memory arrays is the ability to develop multi-turn coils of rather complex structure. A "2V" type coil weave pattern is illustrated in figure 2.0-2. Two features of this pattern are particularly noteworthy; first, some warp lines are left unconnected to provide controlled spacing within and between the word coils, and second, the separate coils are formed by series connection of warp lines.

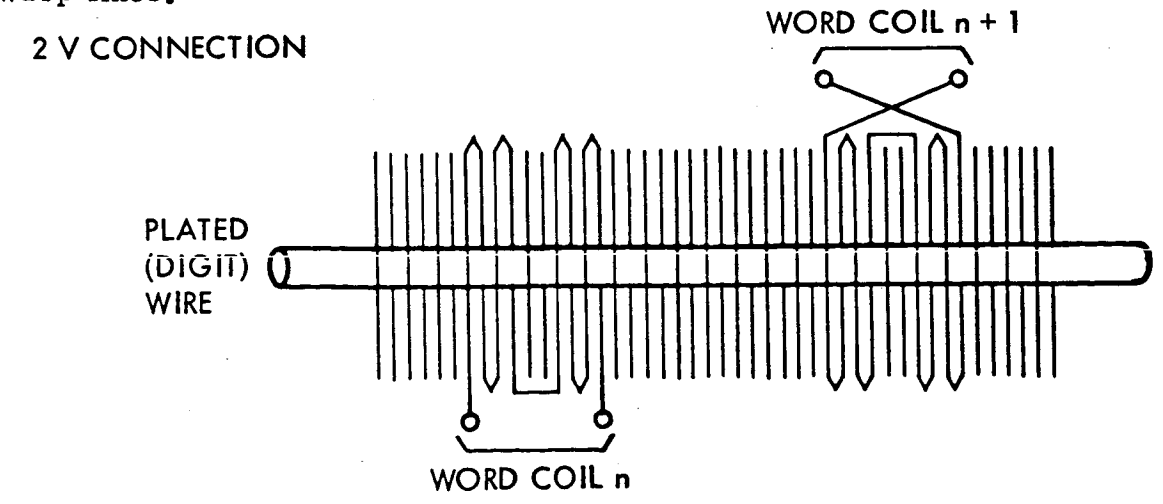


Figure 2.0-2. 2V Word Coil Configuration

These two features permit economical "shaping" of drive fields. The ability to produce shaped drive fields is important. It contributes to intra-cell drive field uniformity as well as to elimination of adjacent cell interaction along the digit line.

The series connection of woven warps to form word coils results in very low word drive current. The "2V" multi-turn configuration requires a word current of 200 ma, which is about one-fourth the current required by a single-turn coil stuch as a strip line, to obtain a corresponding output signal level.

The aggregate effect of the ability to "tailor" the drive fields is to obtain a very efficient realization of the input versus signal versus density potential of the plated wire magnetic structure.

The storage element in the plated wire memory is in ring form with a closed magnetic circuit. External influences or disturbances from adjacent bits have negligible effect on the remanent state. Further, with the information-bearing magnetic flux ring intimately enclosing the sense conductor, as in the plated wire, nearly perfect coupling is achieved. This efficient arrangement results in high read-back voltages and a stable NDRO mode.

2.1 PRINCIPLES OF OPERATION

Woven thin-film memory planes are available for both destructive readout (DRO) and nondestructive readout (NDRO) operation. Within the NDRO group, both unequal and equal word read/write current versions are available. The advantage of the NDRO type is, of course, that no "restore" operation is needed after read. Cycle time and power consumption are minimized. The advantage of the equal word read/write type is that data at unselected digit locations are not altered by word write currents. More economical memory system organizations are therefore possible. The memory plane in the low-power space memory system is both a NDRO and an equal word read/write type.

The following is a brief qualitative description of the operation of plated wire memory planes.

In writing, the word drive current (I_w) in the insulated wires rotates the magnetization in the field from the easy toward the hard direction as shown in figure 2.1-1. Digit drive current (I_D) in the plated wire then tilts the magnetization vector away from the hard direction. When the word current is removed, the magnetization vector rotates to the easy axis in the direction determined by the polarity of the digit drive current. The two binary storage states consist of the two possible directions of the easy-axis magnetization, with selection made by the titlting effect of the digit current, which is removed last.

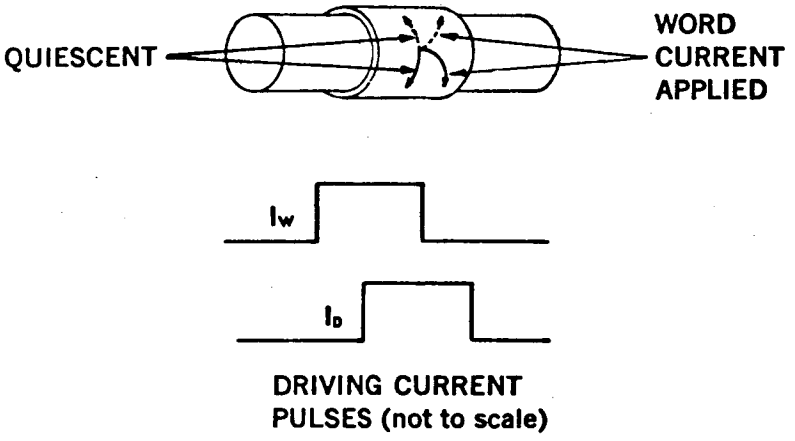


Figure 2.1-1. Write In Process

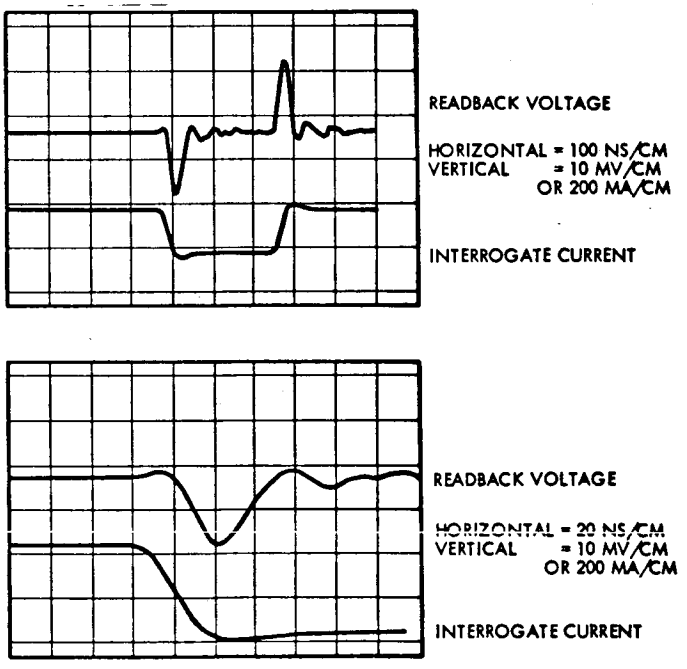
The memory is interrogated by pulsing the word lines. This rotates the magnetization in the plated wire to the hard direction, inducing a voltage in the plated wire which now serves as the sense line. The polarity of the sense voltage depends upon whether the original easy-axis magnetization was clockwise or counterclockwise.

In NDRO operation the magnetization vector rotation is limited so that it falls back to its original orientation upon conclusion of the read pulse.

Data are retained through a read cycle. In DRO operation, where the plane characteristics are not held to the same degree of uniformity and higher interrogate pulse amplitudes are used, the magnetization vector may split, part falling to its original position, and part falling 180 degrees from its original position, so that the information content is destroyed.

In equal word read/write NDRO operation, magnetization vector rotation is limited during write as well as read to the NDRO interrogate value. This limiting has the advantage that data at unselected (i.e., where no digit current flows) bits are left unaltered. Memory system organizations with conditional digit write are thereby possible, and as a result more efficient, more nearly "squared" and/or bit serial selection systems can be arranged. A bit serial system is used in the low-power space memory.

Wave shapes of the interrogate and read-back pulses for a typical woven plated-wire memory plane are shown in figure 2.1-2. The second photograph shows a portion of the first, expanded five times in the horizontal (time) direction.



(DIGIT WRITE CURRENT = 100 MA, DIGIT DISTURB CURRENT = 120 MA, NO. OF DIGIT DISTURBS = 25,000, ADJACENT WORD DISTURBS = 500 MA, NO. OF ADJACENT WORD DISTURBS = 12,000 ON EACH SIDE.)

Figure 2.1-2. Typical PWM Waveforms, MX-W32D64(80)-2VNN Plane

2.2 THE WIRE PLATING

The process of depositing a magnetically soft metal on the surface of a copper alloy wire has been extensively explored at Librascope, and at many other laboratories. The process is currently being commercially exploited in the high volume fabrication of memory planes by Librascope and by several other manufacturers. The basic process consists of depositing a nickel-iron alloy or a nickel-iron-cobalt alloy on the suitably prepared surface of a resilient copper alloy wire. A schematic of the process steps is presented in figure 2.2-1, and a photograph of a pilot plating line at Librascope is shown in figure 2.2-2.

Memory element preparation consists of the following steps. The wire base is first carefully cleaned to remove all organic contaminants. The wire may then be electropolished to remove structural defects due primarily to the drawing operation. Controlled acid etching removes the residual oxide layer and prepares the surface for copper-plating, which provides the necessary homogeneity and surface structure for the magnetic plate.

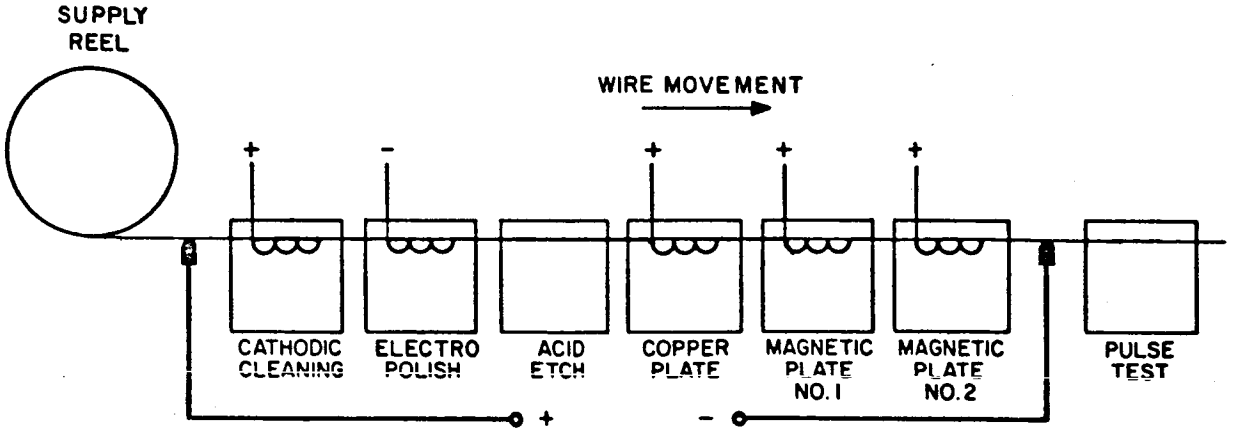


Figure 2.2-1. Plating Line Schematic Diagram

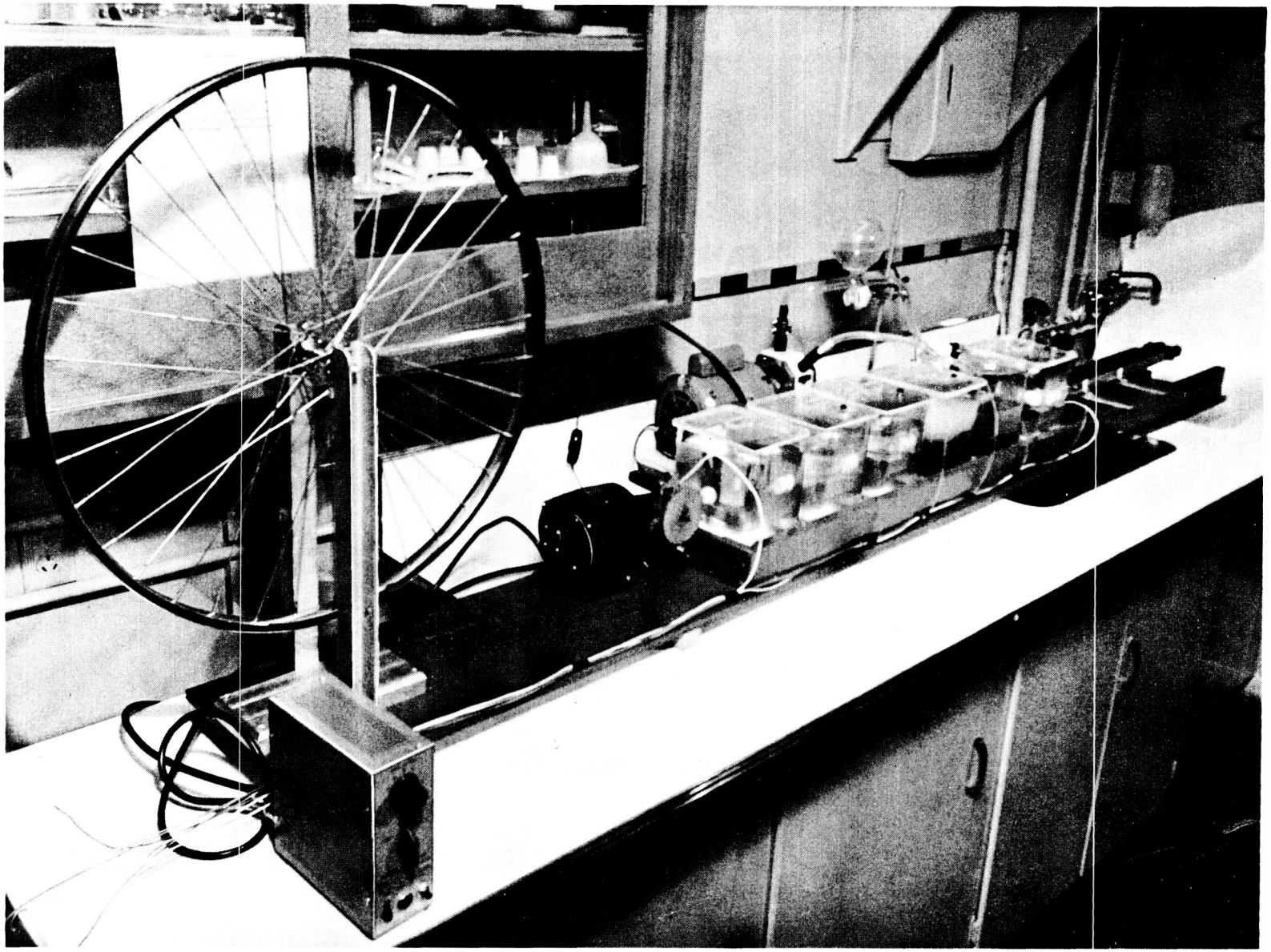


Figure 2.2-2. Pilot Plating Line

The present Librascope plating process incorporates a second magnetic layer plated in direct contact with the permalloy. Layered magnetic structures of certain thicknesses behave as a single homogeneous film. The process of layering permits the tailoring of such properties as coercive force and anisotropy field.

One of the advantages of the wire plating process over other batch fabrication techniques is that it is continuous. Magnetic properties are monitored within a minute or two after the memory layer is formed, and can be closely controlled. The continuous nature of the process permits noting of slow drifts away from optimum magnetic characteristics and quick detection of the results obtained from corrective measures taken to bring the magnetic characteristics back into the optimum range.

A second factor of importance to the high yield obtained in plated magnetic-wire memory elements is the moderate lengths of wire needed for insertion into a memory plane. High yields and consequent economy can be obtained because many short lengths of good wire can be readily cut from the plating run with minimum scrappage for bad spots.

2.3 WEAVING

The woven memory plane is formed on a loom by running soft, thin, (0.002-0.003-inch) insulated copper wires as the warp. Every second warp line is raised and a permalloy-plated beryllium copper wire is inserted as the woof. The positions of the warp lines are then reversed and the process is repeated. Figure 2.3-1 shows the parts of the loom which are significant in the understanding of these operations.

A major problem in making a memory plane in this fashion is maintenance of low stresses on the plated woof wires. Special looms have been developed which create very low, carefully controlled stresses.

2.4 PLANE SPECIFICATIONS

Standard proven Librascope woven plated-wire memory plane designs displaying a wide range of characteristics are currently available. Several

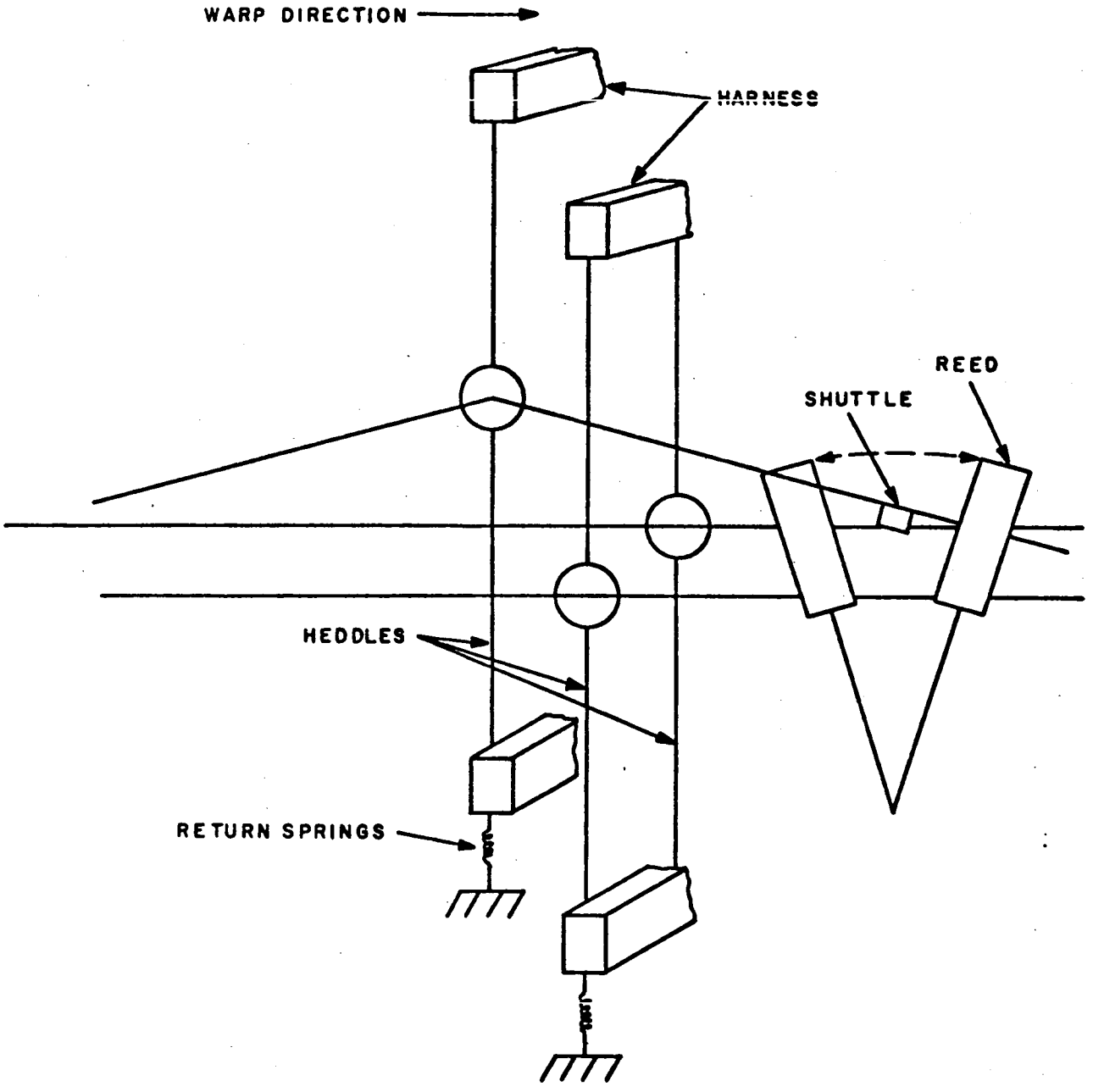


Figure 2.3-1. Significant Parts of Loom

of these offer NDRO, high density, and low-drive properties suitable for space memories. The 2VNN configuration was selected from among these as most suitable for the present program. It has characteristics particularly well matched to the application.

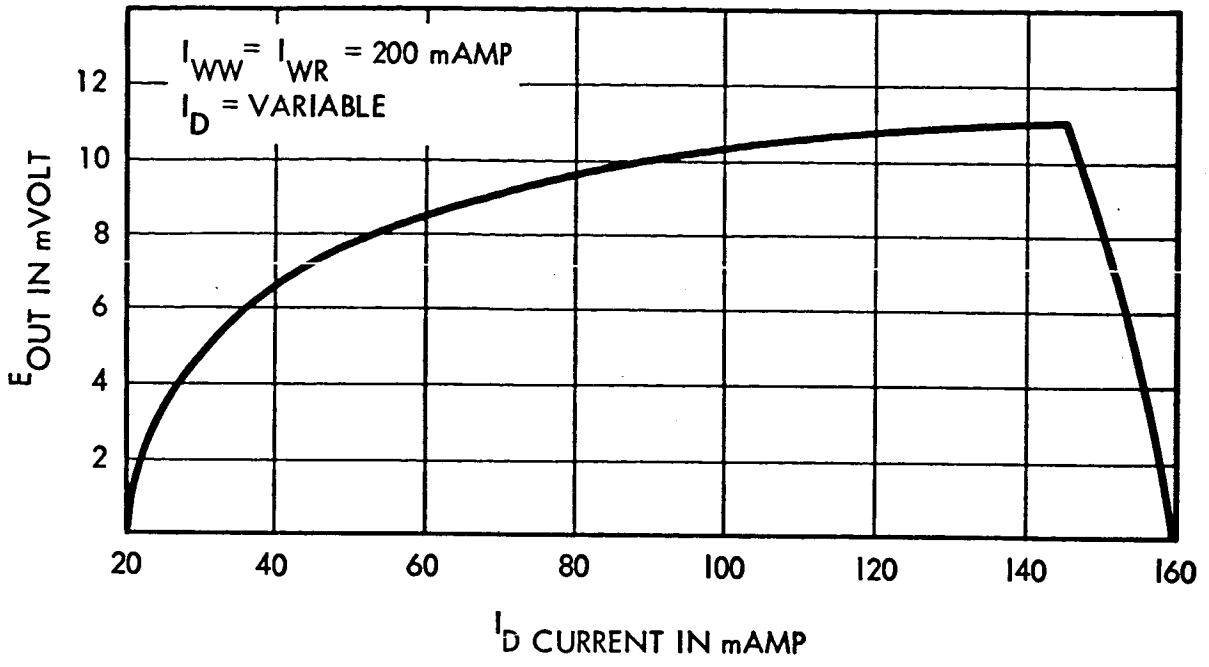
The 2VNN memory array represents an evolutionary improvement over older designs. It has characteristics which permit it to be operated in a NDRO mode using equal word current for reading and for writing. It features extremely low drive currents. Word current is 200 ma; digit current is about 85 ma. All critical aspects of the array design have been proven by experiment and prototype.

The memory plane has a 64-bit by 64-bit capacity. One plane comprises a breadboard system memory stack. The plane is developed of two independently fabricated 32-bit by 64-bit woven plated-wire memory "mats." The two mats are mounted, and encapsulated, one per side on a rigid board to form a plane. Each plane assembly, complete with selection diodes, forms a stack module with dimensions approximately 3.5 inches by 5.5 inches by 0.15 inches. A photograph of the stack module, on a mounting plate, is shown in figure 4.3-2.

Each mat of the breadboard stack module is a 32 by 64 Librascope/Toko standard memory array designated MX-W32D64(80)-2VNN. It is pertinent to note that the MX-W32D64(80)-2VNN design was developed specifically for spacecraft application.

Testing of a MX-W32D64(80)-2VNN plane yeilded cell characteristics typified in the drive current versus output signal plots of figure 2.4-1. Attention is called to the very low, 200 ma, word drive current of the I_D versus E_o curve. It is noteworthy that data for the curves of figure 2.4-1 were taken under the extremely rigorous worst-case test pattern conditions of figure 2.4-2 In that test pattern α, β, and γ are tolerances (in this case equal to 10 percent).

Basic performance and configuration specifications for the two woven plated wire memory mats used in the breadboard space memory stack are summarized in Table 2-1.



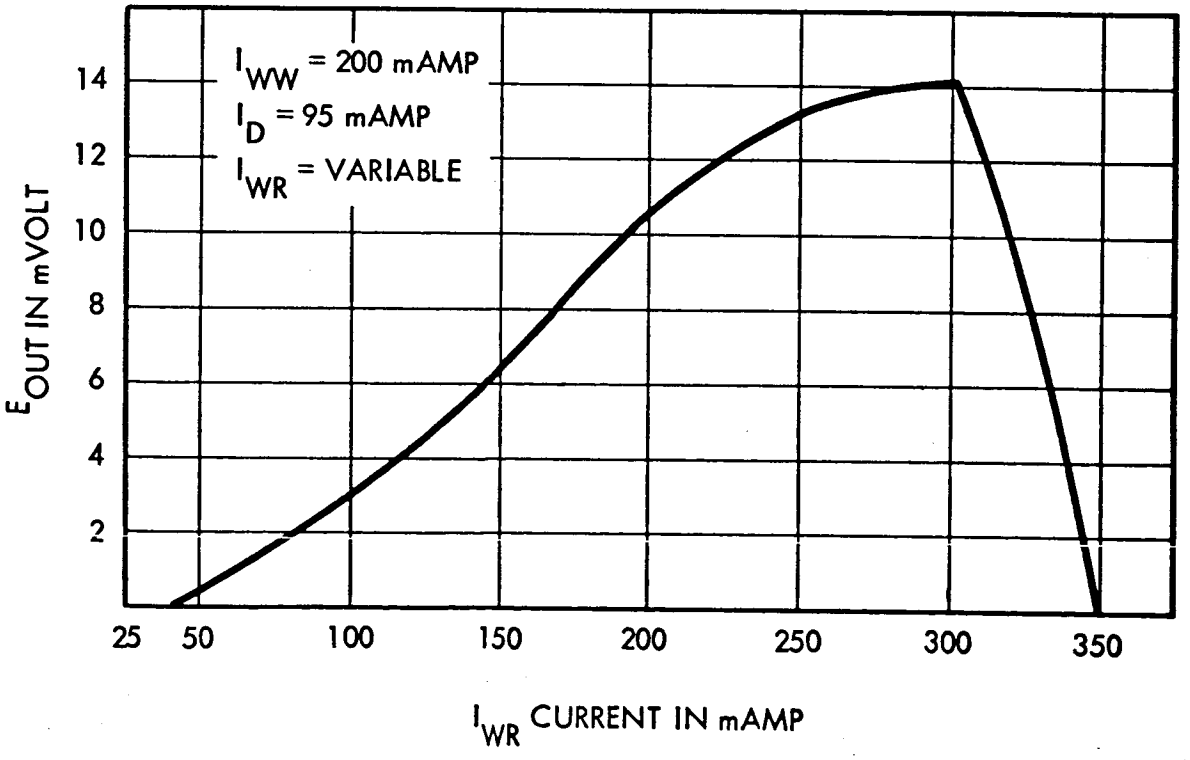


Figure 2.4-1 Characteristics of Memory Plate MXW32D64(80)-2VNN

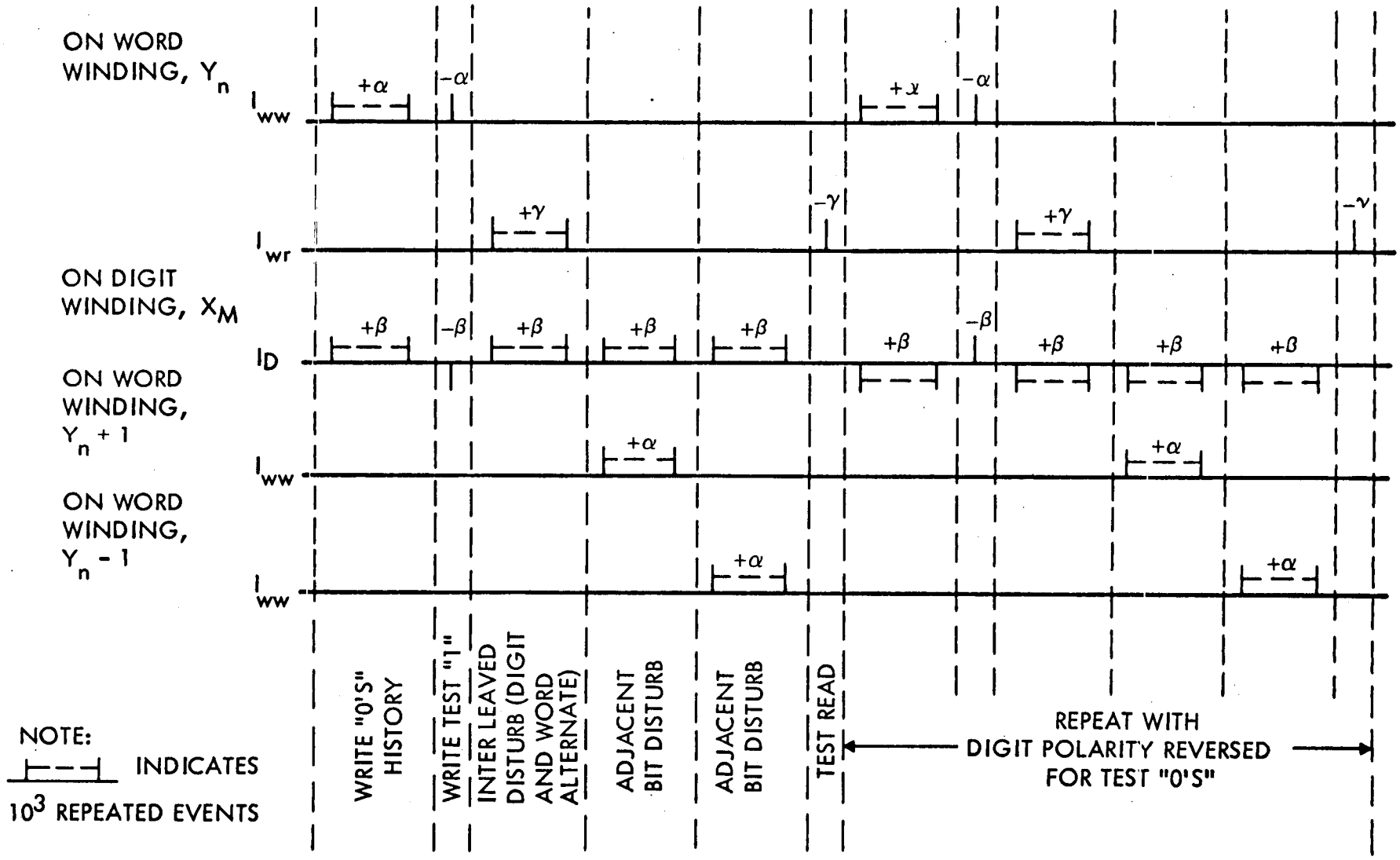


Figure 2.4-2 PWM Test Pattern

Table 2-1. Woven Plated Wire Memory Mat Specifications
Breadboard Space Memory Stack

Model: MX-W32D64(80)-2VNN

Weave

Pattern: 2V (see figure 2.0-2)

Word winding pitch: 0.080 in.

Digit wire pitch: 0.040 in.

Digit wire diameter: 0.008 in.

Capacity

Digit: 80 wires (64 plated and 16 unplated) grouped in sets of five. Each set consists of four plated active wires and one unplated dummy return wire. The unplated wire is located in the center of each set.

Word: 32 words total arranged to terminate 16 word windings per edge on two opposite edges of the mat.

Operating Mode

NDRO with word current for read equal to word current for write. (Designated by the two letters NN at the end of the plane model number.

Electrical Properties

Digit current: +85 ma nominal to write "1"
-85 ma nominal to write "0"

Word current: 200 ma nominal for both read and write.

Digit current tolerance: ±10% nominal.

Word current tolerance: ±5% nominal.

Current compensation: Linear for both digit and word.

Exact current specifications:

Axis	+85°C		25°C		-10°C		
	Maximum	Minimum	Maximum	Minimum	Maximum	Minimum	
Digit	82.5	67.5	96.8	79.2	104.5	85.5	ma
Word	241.5	218.5	215.3	194.8	171.2	154.9	ma

Minimum output signal: ±2.5 mv for an interrogate current risetime of 45 nsec after a standard test pattern which incorporates the following steps performed with all drive parameters at their most unfavorable limits:

a) 1600 event precondition

b) Single event test write

c) 1600 event interleaved disturb

d) 1600 event adjacent cell disturb on each adjacent cell

e) 1600 event test read.

Section 3

MEMORY SYSTEM

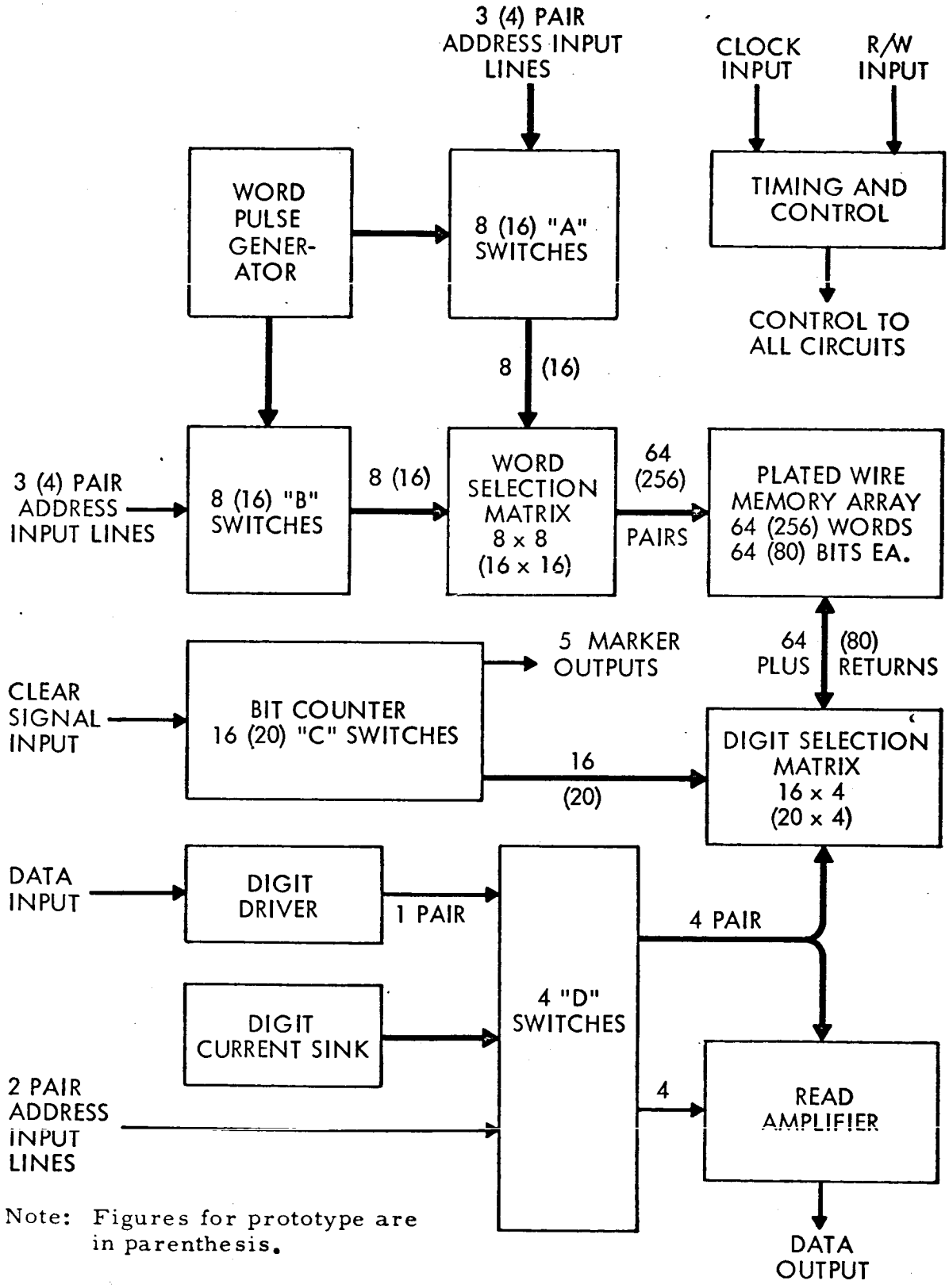
3.1 MEMORY ORGANIZATION

The breadboard memory unit is a random-word-access bit-serial memory, organized to store 256 system words of 16 bits each. The prototype unit will have 1024 words of 20 bits each. The breadboard system is shown in block diagram form in Figure 3.1-1.

The breadboard memory system is internally organized around a memory stack of 64 words of 64 bits each. Advantage was taken of the nondestructive readout and nondestructive word write current features of this memory to reduce the number of word lines that would otherwise be required.

The memory operates in true bit-serial mode sharing a single read amplifier and single digit driver over all digit lines. A 4 x 16 digit-select transformer matrix, described in Section 3.5.1 commutates the read amplifier and digit driver over 64 plated digit wires. To access one of 256 by 16-bit system words, (1024 by 20 bits in the prototype unit) three of eight address bits are decoded to select one of eight A switches; three other bits are decoded to select one of eight B switches. This selects one of the 64 memory-stack words through an 8 x 8 word matrix. The remaining two address bits are decoded to control one axis of the digit-select transformer matrix through the D switches, thereby selecting one of four JPL words within the addressed stack word.

Bits are addressed sequentially by the remaining axis of the digit-select matrix under control of a 16-stage bit counter. The bit counter is advanced by externally-supplied clock pulses. For each clock pulse a read or write operation is performed on the bit designated by the bit counter. At the end of the operation, the bit counter advances automatically to the next bit position; it then remains in standby until the



Note: Figures for prototype are in parenthesis.

Figure 3.1-1. Memory Breadboard System Block Diagram

next clock pulse. When the counter has reached the sixteength stage, the next clock pulse will advance the counter to the first stage. The bit counter may be set to bit 1 from any position by an externally-supplied clear signal.

3.2 SEQUENCE OF OPERATION

Reference will be made to Figures 3.2-1 and 3.2-2 in describing the operating sequence of the memory unit. The sequence begins with a Clear input signal (now shown in the timing diagram) after power has been applied to the system. The Clear signal will set the first flip-flop in the bit register to a standby-ready state. This signal is required only after power has been interrupted or when it is desired to reset the register to bit 1 from any position.

The operating cycle Read or Write begins with the detection of an outside clock pulse. It is necessary to select the desired address and to set the Read-Write command line before the arrival of a clock pulse.

A set of timing pulse generators are provided with the memory unit, described in detail in Section 3.8.1, to provide the sequence of switching actions needed to access the memory and to produce the required output signal waveforms.

The memory unit is in a low-power standby state until a clock pulse is detected. At the detection of the leading edge of the clock pulse the appropriate timing generators are activated. A power pulse from the voltage regulator switch is supplied to the word switches (A and B) and the digit D switches for one microsecond. At the same time, a 1.6 microsecond bit marker pulse is started. The bit marker timing generator also operates the bit counter control circuit to provide high current output drive capability through the bit register flip flop that is in the ready state.

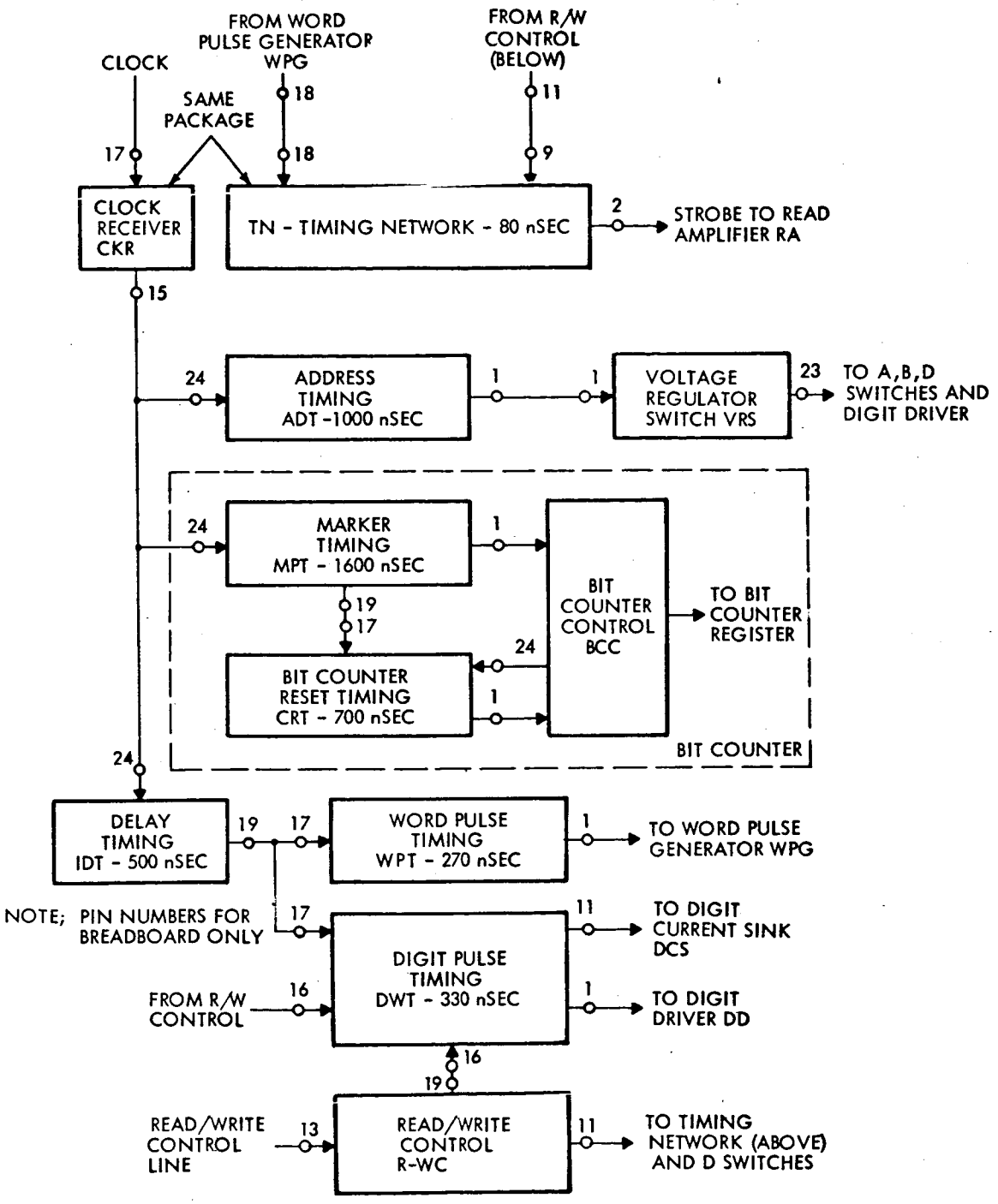
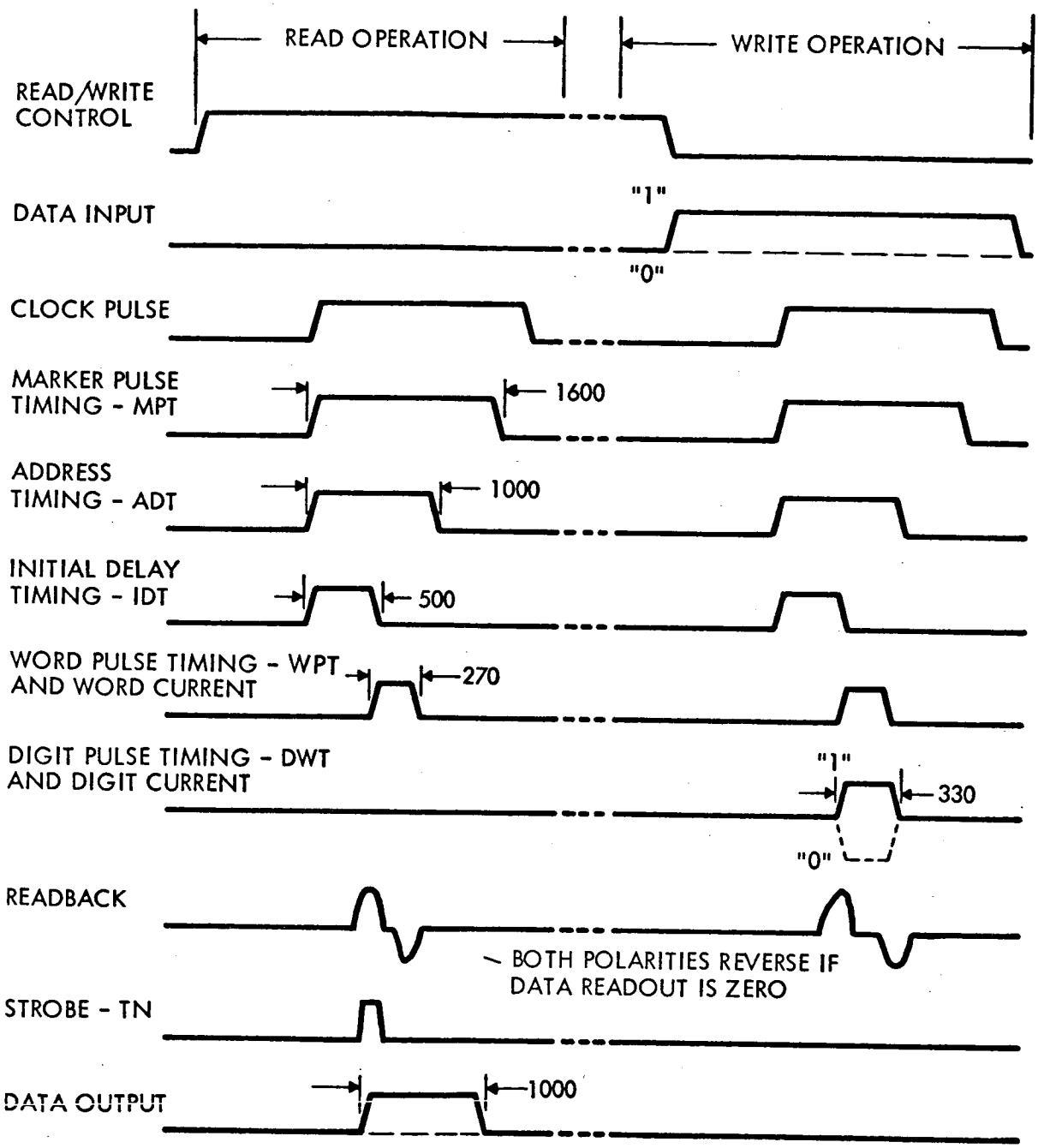
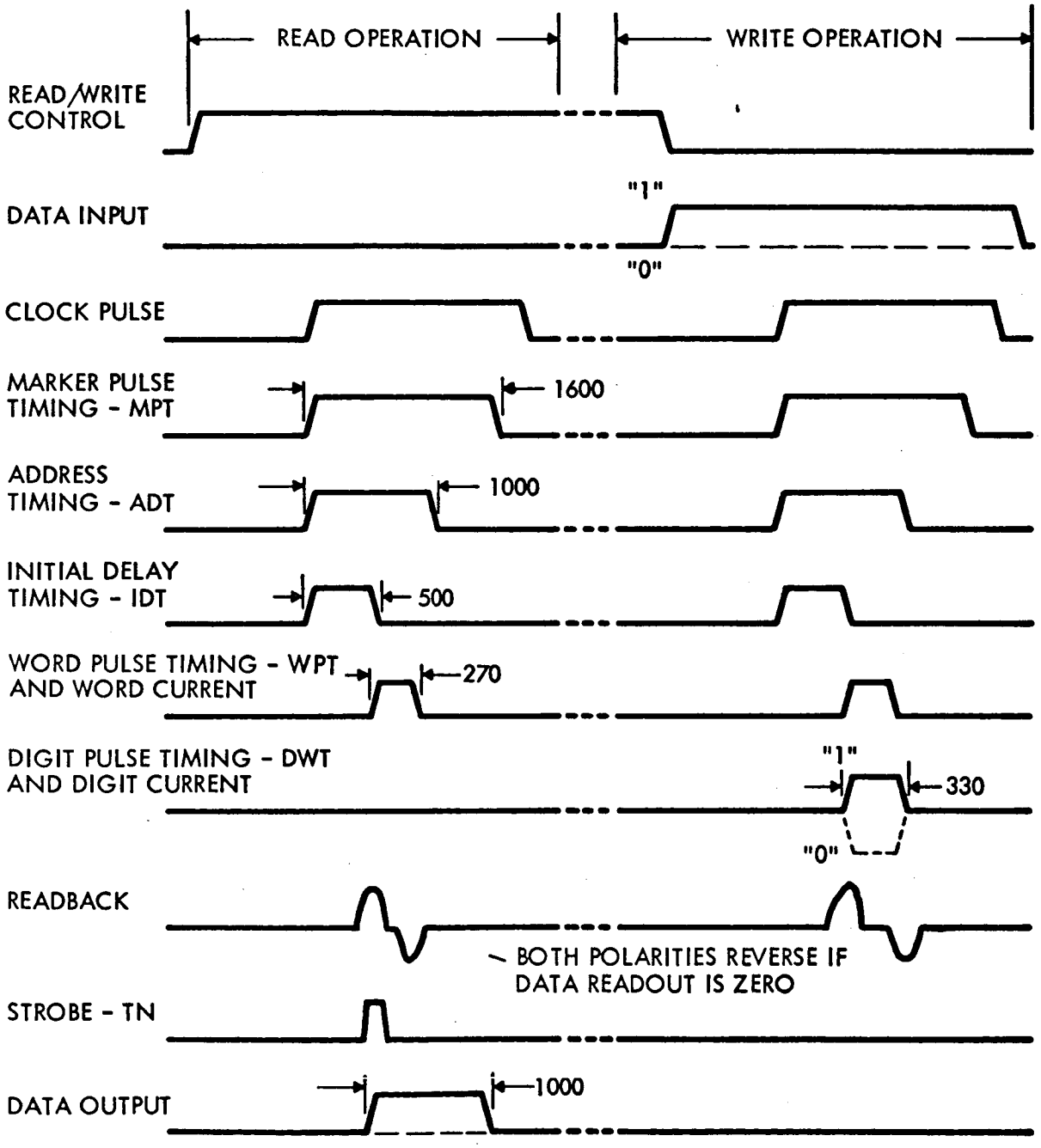


Figure 3.2-1. Timing Block Diagram



NOTE: SEE PULSE WIDTHS IN NANOSECONDS.

Figure 3.2-2. System Timing Diagram



NOTE: SEE PULSE WIDTHS IN NANOSECONDS.

Figure 3.2-2. System Timing Diagram

4. Each A switch line will connect to 16 word diodes instead of 8 and capacitance will be increased by about 8 picofarads. This increase tends to slow the rise time of word pulse and thus reduce readback signal amplitude. However, 8 picofarads is a very small capacitance, and it is anticipated that total A line capacitance will be reduced by at least 8 picofarads because of the shorter lead lengths in the prototype.

5. The word pulse generator output busses will each connect to 16 A or B switches instead of 8. Additional capacitance due to the additional unselected switches will tend to slow word pulse risetime and slightly reduce the readback signal amplitude. Again, it is expected that this increase will be partially or fully compensated by shorter wire lengths in the prototype.

6. Each D bus pair in the digit selection matrix has 20 transformers instead of 16. This will result in slightly higher capacitances on the D busses; however, the effect will probably be cancelled by reduction of woring capacitance in the prototype package.

7. The common control lines to the bit register from the bit counter control circuit will connect to 20 flip flops instead of 16. Unselected stages contribute only capacitance, and the capacitance added by the additional stages in the bit register will be cancelled by reduction in wiring capacitance in the prototype.

8. Unselected A, B, C and D switches draw no power on standby, and standby power is unaffected; however, unselected A and B switches do draw power when the memory operates. At maximum speed (READ or WRITE), power dissipation will be about 6 milliwatts (or 3 percent) higher for the prototype.

A 500 nanosecond delay interval is allowed for all switches to settle. The word pulse generator then generates a current pulse, 200 ma in amplitude and 200 nanoseconds in duration, to drive the appropriate word line through the selected word switches (A and B).

If a Read operation is required, a read gate in the selected D switch is activated to forward-bias diodes in the digit selection transformer matrix and open a transmission path between a digit line and the read amplifier. The timing network generates a strobe pulse for the read amplifier in coincidence with the arrival of the readout signal from the plated digit wire. This readout signal is generated by the leading edge of the word current pulse. If the signal polarity at strobe time indicates a ONE, a one microsecond data output pulse is immediately started. No data output pulse is generated for a ZERO.

If a Write operation is specified, a 300-nanosecond digit-current pulse is generated in coincidence with the word-current pulse. Polarity of digit current is determined by the sense of the binary bit to be stored, as indicated by the voltage level of the data input line to the digit driver. The digit driver will drive the current pulse through the selected D switch and digit matrix transformer and through the appropriate plated digit wire. Shortly after the termination of the word and digit current pulses, power is removed from the A, B, and D switches. The bit counter advances on the trailing edge of the bit marker pulse and all circuits return to standby condition.

3.3 SYSTEM ELECTRICAL SURFACE

This section describes the electrical requirements for power and signal lines connecting to the breadboard and prototype memory systems from external equipment.

Power

DC power must be supplied to the memory system at three levels:

Nominal Voltage	Limits	Maximum Load
+ 15 volts	+ 13.5 to + 16.5 volts	8 ma
+ 5 volts	+ 4.5 to + 5.5 volts	60 ma
- 3 volts	- 2.7 to - 3.3 volts	20 ma

In addition to three wires carrying these power supply voltages, a common return connection is required. The common return is grounded to the memory chassis (or enclosure).

The memory cannot be expected to function properly if power supply voltages go outside the limits given above, even transiently. However, filter capacitors on the power busses within the memory unit will prevent memory circuits from seeing very short transients. These capacitors, probably supplemented with line filter chokes in the prototype, will also remove high frequency components of load current generated by the memory.

Input Signals

The following binary digital signals are required from external equipment. Signal levels are compatible with most of the common saturated logic elements available as integrated circuits (see below).

Function	Number of Connections and Description
Address	Eight bits required on eight complementary pairs of lines for the breadboard, ten for the prototype.
Data	One bit on a single line for WRITE operations. High for "1", low for "0".
Read/Write Control	One line. High for READ, low for WRITE.
Clear	One line. A pulse to the high level for a minimum of 1.2 microseconds sets the memory bit counter to bit 1.
Clock	One line. A pulse to the high level for 500 to 3000 nanoseconds causes a memory operation.

Clock and clear signals must not be given simultaneously. See Section 3.7 (Bit Counter), Specifications.

The address, data, and read/write control signals must be held stable for a minimum of 1.0 microsecond, starting at the leading edge of a clock signal.

Output Signals

The following binary digital signals are generated by the memory unit and are available for connection to external equipment. Signal levels are compatible with most of the common saturated logic elements available as integrated circuits (see below).

Function	Number of Connections and Description
Data	One line. A nominal one-microsecond pulse to the high level starting 600 nanoseconds after the leading edge of the clock input signal indicates a "1" has been read from memory. This line remains at standby ground level for a "0".
Bit Markers	Five lines connected to five different stages of the memory bit counter, as stages selected for the application. A nominal 1600 nanosecond pulse to the high level on one of these lines, starting within 200 nsec of the leading edge of a clock signal, indicates that the memory is operating on the bit address which is marked by that line.

Logic Signal Interface Compatibility

Logic signals, both in and out, for the memory unit are compatible with most common DTL and TTL forms of integrated circuit logic elements. These include:

Fairchild 930 Series DTL

Signetics 100 series DTL

Signetics 400 Low Power Series

Signetics 800 Series TTL

Texas Instruments Series 54 and 74 TTL

Texas Instruments Series 53 and 73 DTL

Texas Instruments Series 1500 DTL

In addition, the memory unit outputs are compatible with Fairchild Low Power Series 9000 DTL. The address, read/write, and data inputs are not, however, because the Fairchild 9000 series elements can sink only 1 ma. at the low level. Compatibility with 9000 series circuits can easily be established by adding input buffer stages within the memory unit if desired. Memory power dissipation will be increased somewhat, but the increase would be minimized by operating the input buffers on a pulsed power supply with a duty cycle proportional to memory data rate and reaching 10 percent at the highest.

Memory output circuits can sink up to 10 ma. at the "0" level while holding voltage within 0.5 volt of ground at the source. They can supply up to 4 ma at the "1" level, which is held to a minimum of 3.2 volts at the source. Output circuits are designed to provide a low impedance drive to the outgoing signal lines at both levels through use of active circuits, rather than power-wasting pull-up resistors.

Memory address inputs will supply 0 to 4 ma, and data and read/write control inputs will supply 0 to 2 ma, to input lines held at the "0" level. None of these inputs require or supply current at the "1" level. Input "0" may range from -0.5 to +0.8 volts as received. Input "1" voltage may range from +2.2 to +6.0 volts as received.

The clock and clear signal input receives sink current from input signal lines held at the "1" level and do not supply current to "0" level lines. While unconventional, this arrangement has permitted zero standby power in the two circuits receiving these signals, which cannot be operated from a switched power supply. The trend is toward "totem-pole" outputs in integrated circuit logic elements, and these outputs are capable of supplying current in the "1" state anyway. Most pull-up resistors in older IC logic elements are also capable of supplying the

small current needed by these inputs. See sections 3.7.3 and 3.8.5 for exact specifications of input requirements for these circuits.

3.4 ELECTRONICS DESIGN PRINCIPLES

System design and circuit configurations were largely completed in the proposal phase for both the breadboard and prototype versions of the Low Breadboard Power Space Memory. Some material extracted from Librascope's proposal (EX 5-1047-BI) is included in this discussion of system design philosophy for completeness. New material includes discussion of circuit design details, component selection and application, and power supply voltages. These topics represent areas of major effort in the phase of the program recently completed.

3.4.1 System Design Goals

As stated in Exhibit I to the contract, the memory unit has these major design goals:

1. Maximum reliability
2. Minimum power consumption
3. Minimum weight
4. Minimum volume

In relation to the electrical/electronic design of the unit, these four goals may be approximated by a single summary goal: minimum component count. This approximation proved valuable in the initial evaluation of the many possible ways of organizing the Memory Unit, although in some instances it was decided that the four primary goals were best served by a configuration which did not minimize component count.

In applying this simple criterion, it was necessary to decide just what constitutes a component. For a first approximation, a single diode, transistor, resistor, capacitor, transformer, integrated circuit, or thin-film resistor network constitutes one component. When a better approximation is needed, competing design schemes must usually be

compared separately for each of the four primary goals. Power requirements may be quickly calculated. Component count still suffices for weight/volume comparisons.

In weighing alternate circuit implementations from the reliability standpoint, we have considered the probability of failure of semiconductors and integrated circuits to be proportional to the total number of connections both inside and outside the case. Thus a monolithic integrated circuit with 10 to 14 leads is more likely to fail than a single transistor by a factor of 3 to 5.

All circuit components are operated sufficiently below rated voltage, current and power levels to make failure due to operating electrical stresses unlikely, considered in relation to probability of failure from defects.

3.4.2 Circuit Design

Most of the memory circuits are switching circuits, and many of these must be designed for discrete or hybrid construction because presently-available monolithic integrated circuits cannot handle the required voltage/current levels.

Two types of circuit coupling featuring negligible standby power dissipation are available in designing these circuits. One type, direct coupling between complementary transistors, is used where relatively long pulse duration is needed. The second, transformer coupling, is used where impedance matching can be utilized to optimize power gain and thus achieve high circuit power gains with a minimum number of components.

Transformers cannot be integrated, yet they may be smaller than a TO-5 transistor enclosure; they have sufficient advantages in this system to justify their use. Physically small transformers can be used because the system requires them to transmit only very short pulses. Repetition rates are low enough for the transformers to recover completely between pulses.

Where transformers are used in interstage coupling, the transformer recovery characteristics are designed and used to sweep away the base storage charge of the transistor being driven. This results in faster switching of the transistor with reduced power dissipation.

Circuits in general have been designed to function under worst combinations of deviations of the following variables:

1. Power supply variations, ±10 percent
2. Ambient temperature, -10° C to +85° C
3. Initial component parameter variation as specified by the vendor
4. Component parameter aging drift, as indicated by Librascope's published Component Application Criteria.
5. Requirements on circuit inputs and outputs.

However, a few knotty "worst case" design problems have been left for Phase II. In all of these cases, breadboard circuits have been built without special selection of components, and have been operated under worst case combinations of power supply voltage and ambient temperature, but complete analytical design may show that the additional assumptions of worst case initial values on all component parameter variables leaves insufficient margins for aging. The following approaches toward solution of the remaining problems are being considered individually and in combination:

1. Regulation of power supply voltage. See Section 3.4.4.
2. Specification of transistor parameters under conditions closer to the application, or with tighter limits. See Section 3.4.3.
3. Use of metal film rather than composition resistors. See Section 3.4.3.
4. Allowing increased power dissipation in the system.
5. Deriving aging margins from the high probability that not all component parameters contributing to a given failure mode will simultaneously reach their worst initial limits.

The last approach will be considered heretical by some reliability analysts and therefore needs elucidation. The prototype and flight hardware circuit modules will not be field-repairable; they will be discarded when they fail to perform within specifications. Circuit acceptance tests on individual modules must be designed to show adequate margins for aging in any event; with the suggested approach there will be a small but non-vanishing probability that a circuit correctly constructed with all component parameters within specified initial limits (but near the unfavorable limits) has to be rejected because of inadequate aging margins. This approach is valid where a failure mode is a function of at least several independent component parameter variations, and is similar to the approach actually taken for monolithic integrated circuits, which are also nonrepairable.

The breadboard memory has no potentiometers or other mechanically-adjustable components. Where a means of adjustment is needed (in the current and voltage-regulating circuits) it is made by soldering in a resistor selected for the particular circuit. No adjustment following the initial one is necessary nor possible in the case of the prototype hardware.

3.4.3 Component Selection and Application

Components have been selected with principal regard to their suitability for the application. Lists of preferred or qualified parts were not consulted. It is intended that all components used in flight hardware will be qualified, but the list of qualified parts for that future time is not yet in existence; components selected for the memory are suitable candidates for that list.

Integrated circuits are used wherever possible; they have very significant size, weight, and reliability advantages and are easy to apply.

More detailed comments on application of the different families of components follows.

3.4.3.1 Transistors. Because of the low power and voltage levels at which the memory operates, power dissipation and collector voltage ratings on transistors are much higher than the levels at which they are used in the system. Current ratings are much higher than applied currents, also; the highest current handled in the memory system is about 250 ma and levels of 0-20 ma are typical. The back voltage ratings on base-emitter junctions has been a problem, however. On diffused silicon transistors, the Veb ratings range from 3 to 6 volts. The interim solution used for the breadboard circuits is to severely limit the current allowed to flow in a reversed emitter junction, usually to a level in the neighborhood of the current used by the manufacturer to test emitter diode breakdown. There have been some recent reports that even very low reverse emitter currents cause gradual degradation of low current beta. For the prototype memory system, either circuit designs will be modified to lower the applied stress to safe limits, or transistors will be specially selected by the semiconductor vendors for sufficiently high emitter breakdown. Most prototype transistors must be purchased on special factory order to have them packaged to TO-46 cases.

Minimum initial beta for transistors is typically given by the manufacturer only for room temperature and a saturation voltage of one volt. These minimums are adjusted downward by circuit designers for cold temperatures, exact collector current, usually a lower saturation voltage, and for old age. Most manufacturers give some data to help in making these adjustments, but every data sheet seems to present this data in a different way. Details on these adjustments for the transistors used in the present system are given in the paragraphs which follow.

At 10 ma collector current and a Vce of 0.35 volts, the 2N2369A has a minimum initial beta of 40 at 25° C and 20 at -55° C. A minimum initial beta of 30 at -10° C is indicated; a cold old age beta of 24 or less has been allowed in most applications.

The 2N3249 has a minimum initial beta of 65 at -10 C for collector currents of 0 to 20 ma and a Vce of 1.0 volts. Data sheet curves

50

indicate that Vce can be lowered to 0.3 volt if beta is decreased to 20 percent; cold old age beta has therefore been set at 40 or less.

The 2N3486A is difficult to apply because guaranteed initial betas are given for only room temperature and a Vce of 10 volts; Motorola's supplementary curves are typical and apply to Vce's of 3 volts or less; nevertheless it is the best available PNP transistor for currents of 100-250 ma. With minimum initial room temperature beta of 100, a cold old age beta of about 40 for a Vce of 0.5 volts has been allowed.

The 2N3736 has a minimum initial beta of 37 at 250 ma collector current, room temperature, and a Vce of 1 volt. Conservative deratings for cold temperature and aging put working beta at 20; no attempt has been made to force Vce lower than 1 volt.

3.4.3.2 Diodes. Most silicon diodes sold in large quantities are built and/or selected to customer's specifications. The breadboard uses the Fairchild FD6331, a high conductance, low capacitance, fast recovery diode selected from the FD600 series to a Librascope specification, in all circuits needing diodes. The FD6331 has a conventional DO-7 glass package. The memory stack uses the Microsemiconductor MC9853 which is electrically similar to the FD6331 but comes in a much smaller package. The prototype will use the MC9853 in all locations. The redundant diode version for the stack is designated MC9962.

3.4.3.3 Resistors. The breadboard memory system has been constructed mostly with 1/4 watt 5% composition resistors. For the prototype, 1/8 watt 5% composition resistors are presently called out. In a few places where high stability is needed, 1 percent metal film resistors are used. It is quite possible that the prototype unit specifications will be changed to call out 1/20-watt metal film resistors exclusively. The 15 to 20 percent end-of-life tolerance usually allowed for 5% composition resistors may prove to cost too much in terms of power dissipation in the course of completing analytical worst case circuit designs. It seems likely that 15 to 20 percent end-of-life

tolerance is too conservative for these resistors in encapsulated cordwood modules with no severe humidity problem, but tests to establish this assumption on firm ground probably cannot be carried out within the scope of the present program.

High unit costs ($2 - $3) of 1/20 watt metal film resistors are not a serious problem for space applications. The disadvantages are that these resistors are not stocked and delivery times are long (3 to 8 months), and that low volume production raises question about the rate of failures from defects. If the prototype unit is fabricated with 1/8 watt composition resistors, this would not preclude changing to 1/20 watt metal film resistors for flight hardware, as they are nearly identical in physical size.

3.4.3.4 Other Electronic Components. Integrated circuits have been used where possible in the breadboard memory. They are applied under conditions well within data sheet ratings.

The capacitors in breadboard circuits are those that were readily available. Tantalum types are used for power line filters, others are ceramic. Electrical requirements for capacitors are easily met; physical size and configuration are of major importance for the prototype and will govern final selection for that unit.

Transformers and the delay line in the breadboard are readily available types. The prototype components will be fabricated to specifications written specially for each application.

3.4.4 Power Supplies

This memory has been designed to work with unregulated DC power supply lines. One reason for this is to eliminate the need for voltage regulators on the supply lines and thereby eliminate the power dissipation associated with them.

Experience with the design of this memory suggests a review of this policy. Although power supply voltage deviations of ±20 percent were

initially contemplated, circuit design became so difficult that the figure was reduced to ±10 percent. Moreover, a major portion of the memory operates from regulated power; the regulators are included in the memory. Current regulators for word and digit currents are needed to establish the current magnitudes compensated for temperature as required by the memory element. A regulator is included for the A, B, and D switches and the Digit Driver because total power dissipation is less than it would be without it.

To see how this is true, consider the designer's problem. He must work with the worst case, or lower limit of voltage in establishing his designs. If the voltage at nominal is 10 percent higher than the minimum and the load is resistive, current rises 10 percent and dissipation rises 20 percent. Most silicon semiconductor circuits, and the present system in particular, include one or more silicon diode voltage drops in the current paths. These drops, about 0.7 volt each, do not change much with current; as a result an increase of 10 percent in power supply voltage causes an increase of more than 10 percent in the voltage of the current-determining resistance in the circuit; current may rise 20 to 30 percent and power dissipation may rise 30 or 40 percent. If a regulator is used, current stays constant and power dissipation rises only by the same percentage as the voltage. In all cases, additional power dissipated by virtue of higher than minimum voltage is wasted power.

Regulation of the +5 volt supply outside the memory system is desirable for other systems using integrated circuits on this same power bus, as well as for the memory. Manufacturers data sheets guarantee performance only for a narrow range of power supply voltage, typically ±10 percent, and regulation of the power bus would increase margins for aging of these circuits. An additional gain in aging margins is obtained if the regulated voltage drops from, for example, +5.5 volts to +4.5 volts as the temperature rises from -10 C to +85 C. All solid state circuits, monolithic and discrete, will benefit from this kind of a curve.

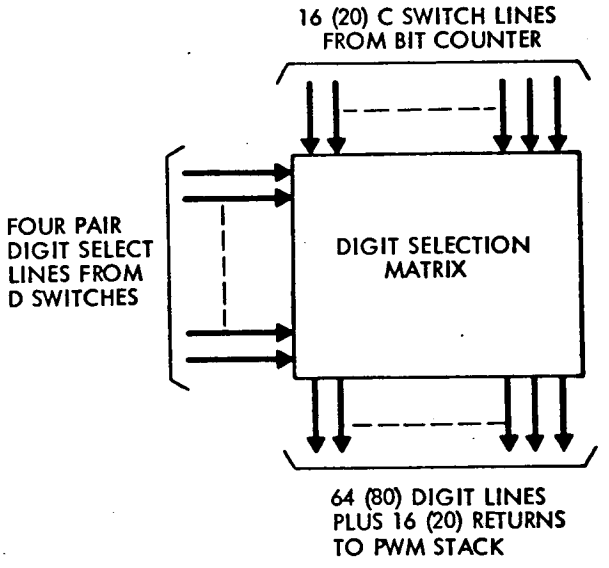
Regulation of the +15 and -3 volt supplies would be advantageous to the memory system also, but the advantages are less significant.

3. 5 DIGIT ELECTRONICS

The digit electronics includes the digit driver, read amplifier, digit current sink, D switches, and digit selection matrix. The bit counter, described in Section 3. 7, contributes the C switch leads which drive one edge of the 3. 7 contributes the C switch leads which drive one edge of the digit selection matrix.

3. 5. 1 Digit Selection Matrix

The Digit Selection Matrix, figure 3. 5-1, provides means of selecting one of 64 plated digit wires during a Write or Read operation (80 wires for the prototype).



DIGIT SELECTION MATRIX ELEMENTARY DIAGRAM

NUMBERS IN PARENTHESIS APPLY TO THE PROTOTYPE SYSTEM

Figure 3. 5-1. Digit Selection Matrix Elementary Diagram

The matrix consists of 64 transformers, one for each digit path, arranged in four groups of 16 (the prototype unit will consist of four groups of 20), as shown in figure 3. 5-2. The secondaries of the 64 (80) transformers are connected to 64 (80) digit lines.

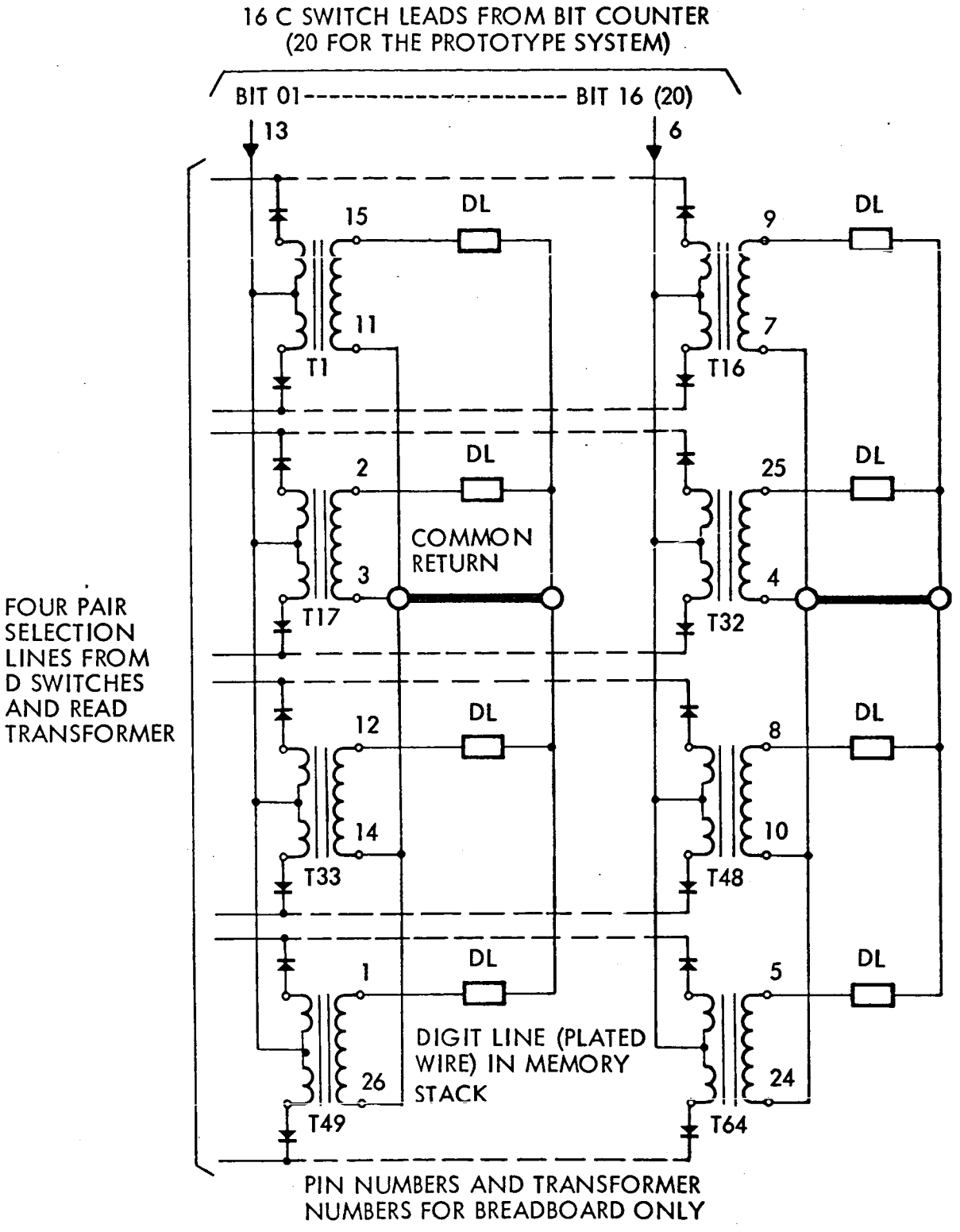


Figure 3.5-2. Digit Selection Matrix Schematic Diagram

One half of the center-tapped primary winding is driven to write a "1", the other half is driven for a "0". Both polarities of output current are thereby obtained from two unipolar primary terminals. Each of the 16 vertical busses in the matrix (figure 3.5-2) connects four transformer center taps to one C switch lead output from the bit counter. Each of four pairs of horizontal busses connects sixteen matrix transformers to a winding on the read amplifier input transformer and to a pair of D switch output transistors. Selection of both is controlled by the D switches, described in Section 3.5.2.

The matrix will pass current pulses of 110 ma with 60 nanosecond rise time and of 400 nanoseconds duration for a Write operation, and low level voltage read signals of 2 mv in amplitude during a Read operation.

Circuit Description

The operating sequence is as follows (refer to figure 3.5-2): for a Write operation, the bit counter puts +5 volts through a low impedance on one of the 16 C switch leads. The D switches select one of the four pairs of digit drive output transistors which connect to one of the four pairs of horizontal busses. When the Write timing pulse appears at the digit driver, current flows from the center tap of the selected matrix transformer into one leg of the selected horizontal bus, the leg chosen depending on whether input data was "1" or "0". The digit current path continues through one of the digit drive output transistors in the selected D switch. At the secondary of the selected matrix transformers, a current pulse is driven down the digit line to a short termination at the far end.

For a Read cycle, +5 volts from the bit counter is again present on one of the 16 C switch leads. One of the center taps of the four read transformer primaries (see Section 3.5.5) is selected by a D switch, which pulls current from the center tap of one of the 64 matrix transformers through the selected primary of the read transformer toward ground. The current places the diodes in a low impedance conducting region. A read signal on the digit line induces a voltage in the selected matrix transformer which is connected to a primary of the read transformer by the horizontal

bus pair. This, in turn, couples the signal into the secondary winding of the selected read transformer which drives the read amplifier.

Design Details

In a plated-wire memory, the digit wires carry both high-level digit drive currents (100 ma) of two polarities and low-level read-back signals (5 mv typical). The digit selection matrix must handle both signals efficiently. This puts stringent requirements on the components used in the matrix, namely, the transformers and diodes.

During a write operation, a selected circuit is required to pass current pulses of 100 ma with 80 nanosecond rise times and 300 nanoseconds duration. The unselected circuits must present a high impedance to this current path so as not to affect the current waveform.

A minimum primary inductance of 100 microhenries will pass this current pulse with good flat-top reproduction when driving the full length of the digit lines in the prototype unit. The diodes in each unselected transformer will provide the isolation if they stary reverse biased under all conditions. When the current pulse is impressed on the digit wire, a voltage pulse will develop across the transformer with an amplitude determined by the amplitude of the current pulse Id, the impedance of the digit line Zo, modified by the ratio of the propagation delay in the digit lines Td and the current rise time Tr.

or $$V = Id \times Zo \frac{2Td}{Tr}$$

Substituting values:

$$V = 100 \times 10^{-3} \times 100 \frac{2 \times 12 \times 10^{-9}}{80 \times 10^{-9}}$$

$$= 3 \text{ volts}$$

The selected vertical bus puts +5 volts on the four transformer center-taps common to the bus. (See figure 3.5-2.) When the upper horizontal bus is driven to write a 1, the voltage on this bus will drop to approximately +1V. (+5V - V - diode drop).

Since all unselected vertical busses are at ground potential, all other diodes connecting to the upper horizontal bus will be reverse biased and will present a high impedance to the selected circuit. The lower horizontal bus of the first pair (common through the driven transformer) will rise to approximately +8 volts (less a diode drop). Here, it is necessary to keep the diode in the read transformer that connects to the lower bus reverse biased. All read transformer center-taps are referenced to +15 volts, thus assuring that all diodes in the read transformers are reverse biased during a Write operation.

During a Read operation, more consideration must be given to the matching of diodes and to balancing the conduction path in order to present low noise characteristics to the read amplifier. The noise generated when a circuit is selected results in a transient caused by unbalanced circuit components and circuit capacitance, including that in the transformer windings. This transient is similar in characteristic to a Read signal, but is terminated 400 nanoseconds prior to the arrival of a legitimate signal on the digit lines.

Another source of noise, resulting in a difference voltage level, is unbalanced voltage drops in diodes. This difference voltage will also cause a current to flow in the selected transformer that couples into the digit wire. Currents flowing in the digit wire will develop a voltage proportional to the resistance of the wire. This voltage will add to the unbalanced diode drop to form the bulk of noise that lasts the entire interval during which this circuit is selected.

For proper operation of the memory, this noise must be reduced to a negligible amount by the time the Read signal appears at the Read amplifier, which is 500 nanoseconds.

This is accomplished in the read amplifier with a differentiating network having a time constant of 0.16 microseconds. After an interval of three time constants the noise level should not exceed 20% of the minimum specified input signal of 2.5 mv. This translates into an equivalent input noise of 10 mv.

Parts Specifications

Part	Breadboard	Prototype
Transformers	Technitro 2XLSA	Pulse Engineering "Flat-tran"
Diodes	Fairchild FD6331	Microsemiconductor MC9853

3.5.2 D Switch (DS)

The D switch (figure 3.5-3) is used to perform two functions. During a Write operation the D switch selects one of the four pairs of digit drive output transistors, which connect to one of four pairs of D buses in the digit select matrix (Section 3.5.1). This permits Write current from the bit counter to pass through the selected transformer in the digit matrix and continue through the output transistor in the D switch and into the appropriate digit line to execute a write operation.

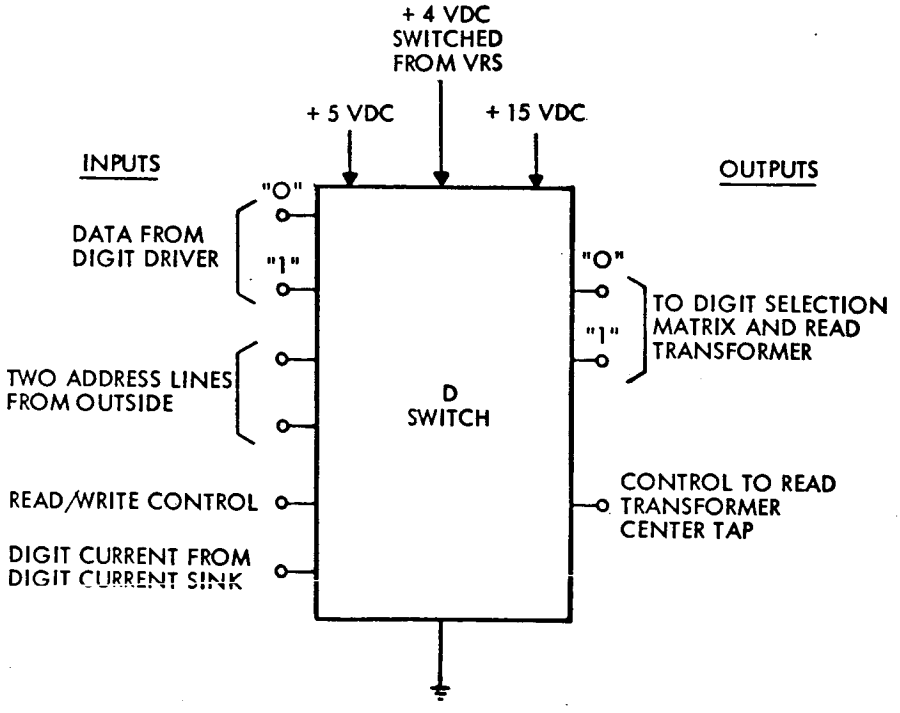


Figure 3.5-3. 'D' Switch Elementary Diagram

During a Read operation the D switch activates a read gate connected to one of four center taps in the primary windings of the read transformer RXF. The four primary windings of the read transformer connect to the D busses in the digit select matrix.

A D switch is selected by the word address lines and is active during a Write or Read operation. Power consumption of this circuit is zero while the memory is in standby. When the memory is in operation, control power is applied through the voltage regulator switch for one microsecond at each clock pulse, thus minimizing the average power drain in the system.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient Temperature, operation: -10° C to +85°C
nonoperating: -10° C to +139°C
Switched Power, +4.3V ±0.2V at -10°C
+3.9V ±0.1V at +25°C
+3.3V ±0.2V at +85° C
Address Input "ON": +3.0 to +5.5 volts
Address Input "OFF": 0.0 to +0.5 volts
Input "Write", +3.8 to +5.5 volts from digit driver
Output "Write", 105 ma maximum
Maximum Pulse Width, 500 nanoseconds
Duty Cycle: 0 to 30%
Input "Read", +4.2 to +5.5 volts from read-write control
Output "Read", Sink 7 ma maximum from read transformer.

Performance: This circuit performs within the limits specified below for all combinations of conditions within the limits specified above.

Power Supply Loading: 1.1 ma maximum on +5VDC supply
1.2 ma maximum on +15VDC supply
2.0 ma maximum on switched +4VDC supply
Power Supply Loading in OFF condition is due to leakage currents only, which are considered negligible.
Address Line Loading (Low): Line sinks 2.0 ma maximum for 1 microsecond.
Address Line Loading (High): Negligible
Output Loading: The circuit will supply a 105 ma current pulse for a write operation and sink a 5 ma current pulse for a read operation.
Turn on Time: Q1 and Q2 will reach 90% of voltage level in less than 200 nanoseconds; Q3 and Q4 turn on time is 50 nanoseconds.

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Turn off Time: Q1 reaches 90% of voltage in less than 0.5 microseconds; Q2 reaches 90% of voltage in 1.0 microsecond; Q3 and Q4 turn off in less than 100 nanoseconds.

Circuit Description. (See figure 3.5-4.)

The operating sequence starts with logic levels on the address lines that back-bias the input diodes. Then, at the sensing of a clock pulse, the voltage regulator switch applies a 4 volt level to the base resistor for one microsecond. Transistor Q1 turns on, pulling the collector voltage to ground level. After a 500-nanosecond delay, allowed for all address switches to settle in the system, a Write or Read operation is executed.

For a Write operation, the write timing generator activates a digit current sink connected to the output emitters for 300 nanoseconds. Simultaneously, the digit driver is turned on for 300 nanoseconds. If the data input line requires a "1" to be written into the memory, a +5 volt pulse from the digit driver appears on the "1" line to cause current to flow in the upper half of the transformer through the limiting resistor and collector of Q1 to ground. A current pulse coupled into the secondary of the transformer is of a polarity to turn on the upper output transistor Q3. With the output transistor turned on, a current transmission path is opened to allow current to flow from the bit counter through a digit selection transformer through the output transistor and into the digit current sink. This writes a "1" into the memory. Conversely, if a "0" is to be written into the memory, a +5 volt pulse appears on the "0" line to cause the output transistor Q4 to turn on. The resulting output current will cause a current to flow in the digit line in the opposite direction through the selected transformer and to write a "0" into the memory.

To perform a Read operation, the transistor Q1 is turned on as above. In addition, a pulse from the read-write control circuit goes to +5 volts to turn on the gate transistor Q2. Currrent now flows from the bit counter, through the digit selection transformer, through the read transformer and into the collector of Q2 and Q1 to ground. This current provides forward bias to isolation diodes in the digit matrix and opens a transmission path to Read signals between a digit line and read amplifier.

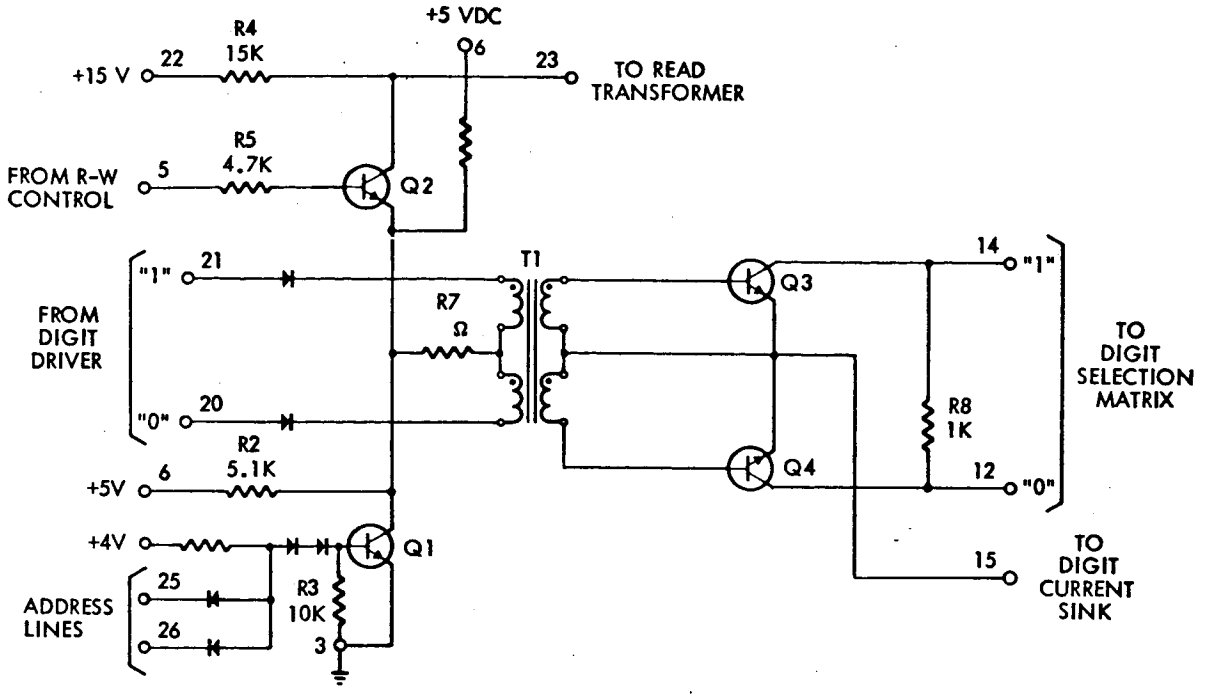

Figure 3.5-4. 'D' Switch Schematic

Design Details

Transistors Q3 and Q4 have a minimum end of life beta of 25 at cold temperature for a Vce of 1 volt. A minimum base current of 4 ma is required for a collector current of 100 ma; 5 ma has been allowed. To this, a transformer magnetizing current (based on the minimum inductance of 160 microhenries) or 2 ma is added to give a required 7 ma of base current. (See figure 3.5-5.)

The limiting resistor R7 is selected to be 220 ohms to make available the minimum required base drive for the worst operating conditions. The total collector current of Q1 during a Write operation is 7 ma, plus 1.0 ma through the collector resistor, or a total of 8 ma with a possible maximum current of 11 ma.

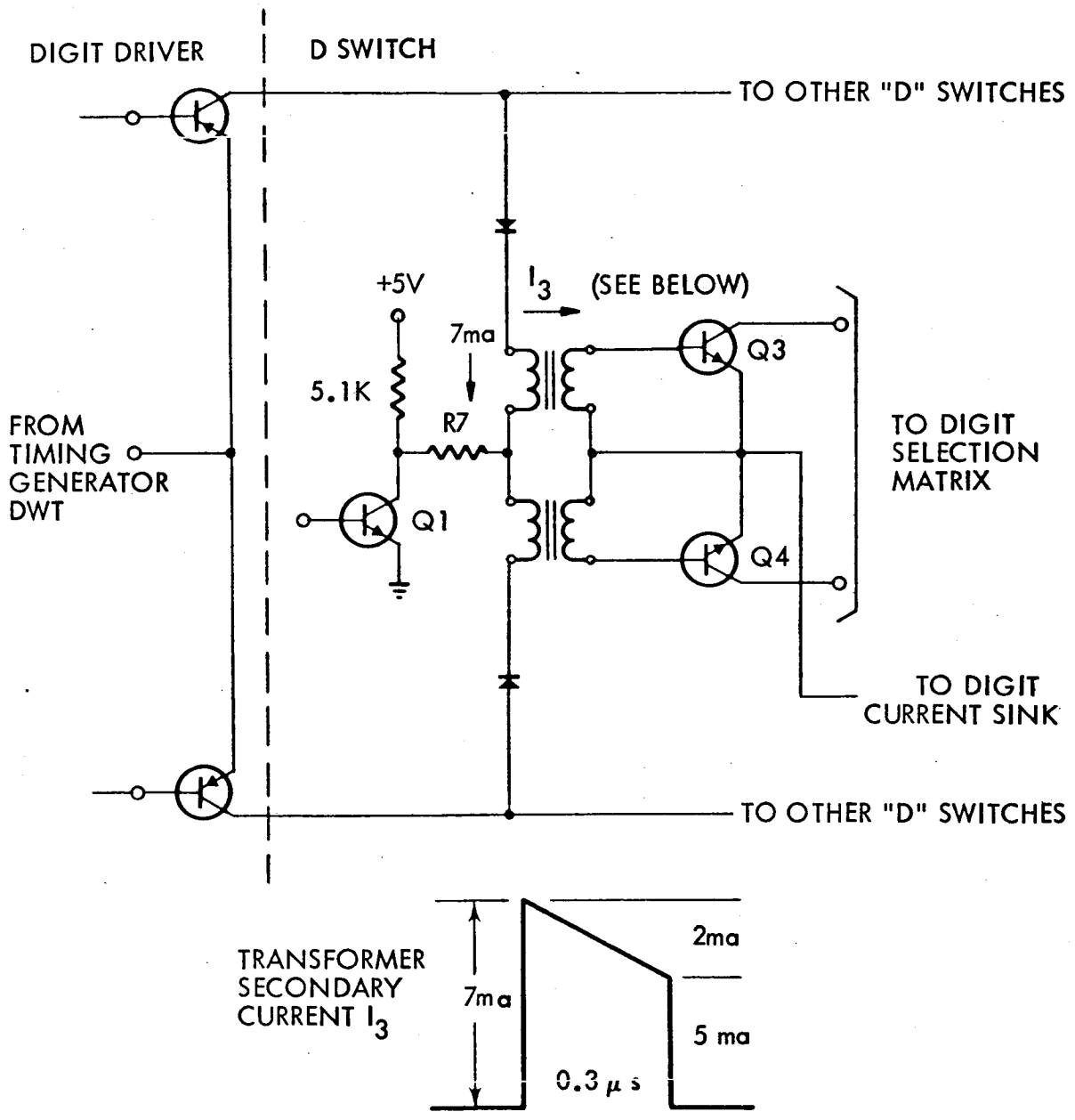

Figure 3.5-5. 'D' Switch Output Stage Analysis

During a Read operation, the maximum collector current of Q1 is 6.5 ma (determined by a limiting resistor in the read transformer). The input stage must, therefore, be designed to handle the higher write current under all operating conditions.

3.5.3 Digit Driver (DD)

The digit driver (figure 3.5-6) is used to provide write information to digit lines in accordance with the data input signal levels. Its inputs are derived from two sources. One source is the computer data line that connects directly to the input of the digit driver. The voltage level on the data line determines whether a 1 or 0 will be written into the memory. The second input source is the write timing generator. This input signal connects to the emitters of the output stages and drives the output transistor that is activated by the input inverter stage.

The write timing generator signal is available only when a write operation is to be performed.

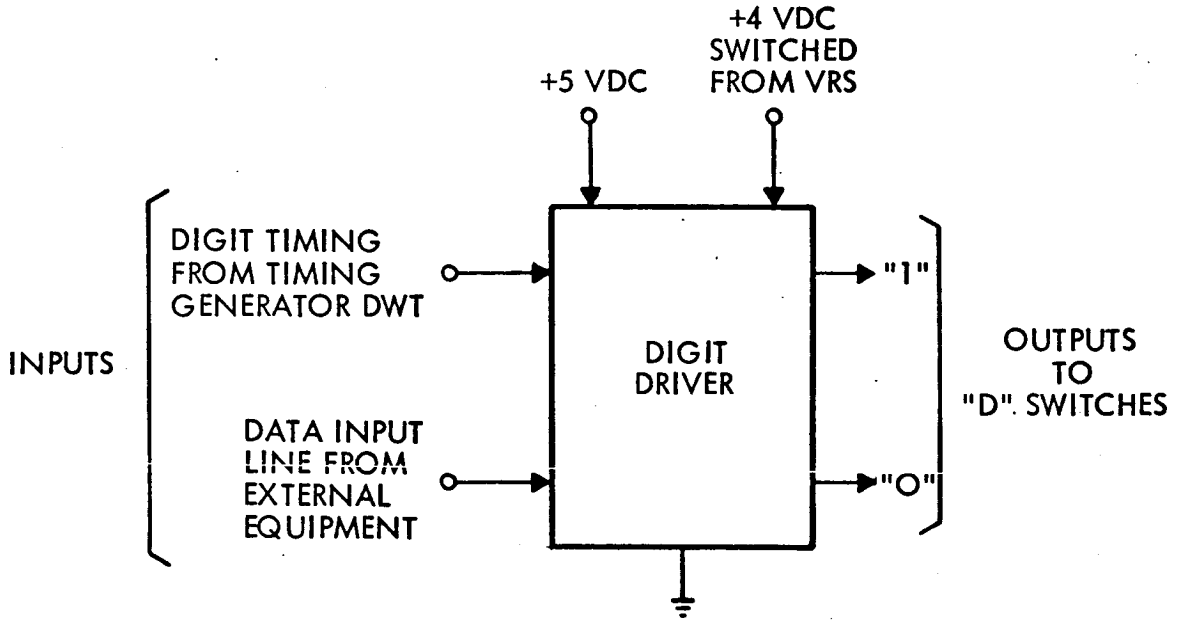

Figure 3.5-6. Digit Driver Elementary Diagram

Circuit Specifications

Conditions:

Ambient Temperature, operating: -10 C°to +85 C°
nonoperating: -10 C°to +139 C°
Power Supply: +4.5 to +5.5 volts DC
Switched Power: +4.0V nominal (voltage regulator switch)
Data Input: "1" = +3.0 to +5.5 volts
Data Input: "0" = 0.0 to +0.5 volts
Timing Input: +4.2 to +5.5 volts
Output Loading: 15 ma maximum
Duty Cycle: 0 - 100%

Performance:

Power Supply Loading, ON Condition: +5V Supply, 1.8 ma maximum
+4V Regulated, 3.5 ma maximum
Power Supply Loading, OFF Condition: Transformer Leakage only
Input Signal Loading, Low voltage state: Input line sinks 1.7 ma maximum
Input Signal Loading, High voltage state: Transistor leakage currents only
Output Current: 15 ma maximum
Response Time: The voltage regulator switch must turn on a minimum of 200 nanoseconds before the write timing generator
Rise Time of Q1 or Q2, measured from the timing generator turn on is 40 nanoseconds maximum
Fall Time is 80 nanoseconds maximum

Circuit Description

The Digit Driver consists of two simple input inverters to generate the true and complement of the input data, and a pair of gated output stages to provide the necessary digit drive into the D Switches. In the following discussion, reference will be made to the digit driver schematic of figure 3.5-7 included in this section.

Two input inverters are contained in a quad 2-input monolithic DTL Nand Gate (Signetics CS720J). These nand gates have no internal collector resistors, making the use of separate collector and base supply voltages possible. In this circuit the +5 volt supply provides collector voltage, and the switched supply from the voltage regulator switch supplies base drive.

In this arrangement the entire circuit consumes no power when the system is in Standby. During operation, the voltage regulator switch supplies base drive for one microsecond out of a 10 microsecond minimum cycle

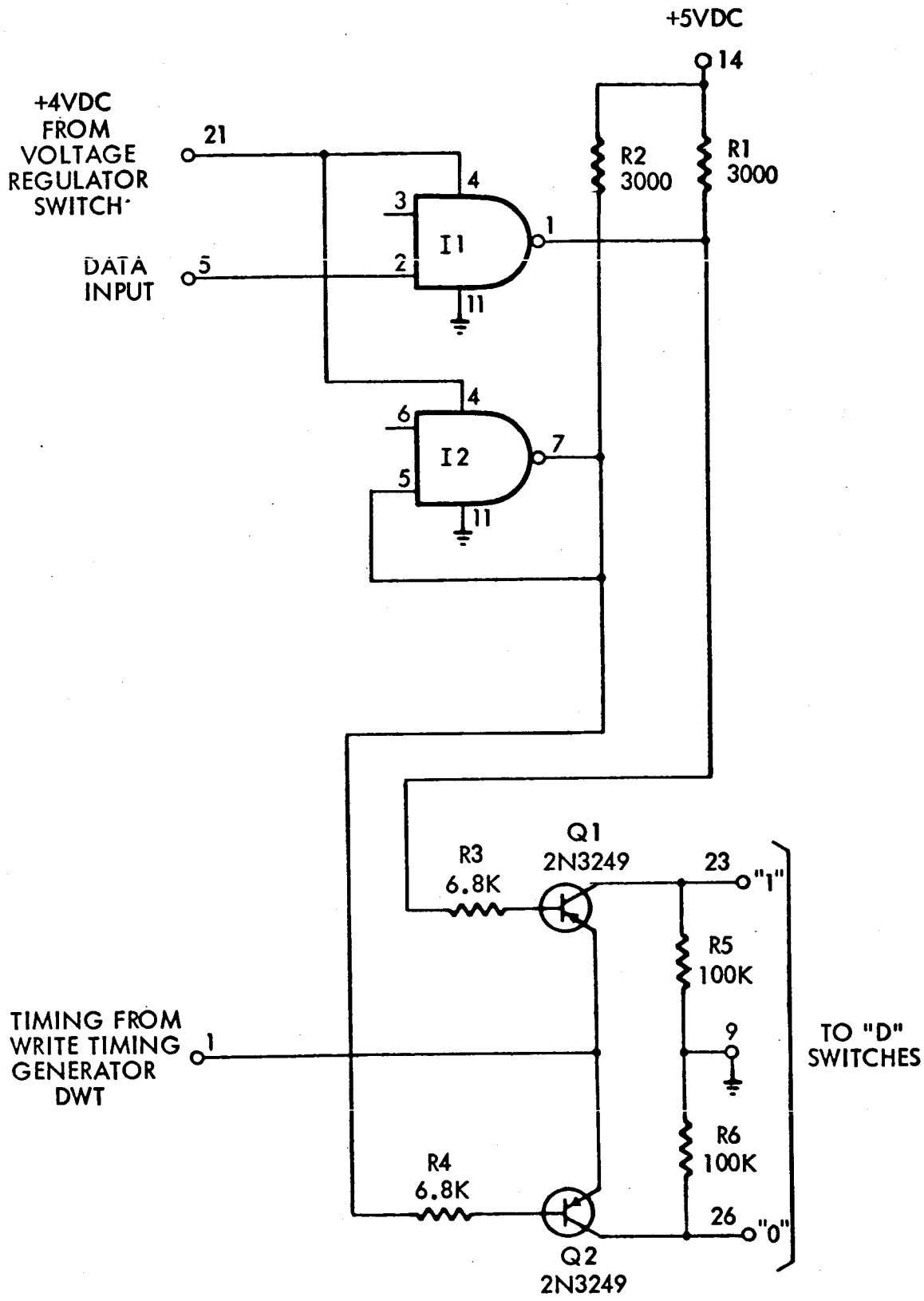

Figure 3.5-7. Digit Driver Schematic Diagram

time, thus minimizing the power drain in the system. When base current is available, the outputs of the inverter stages assume the proper logic levels as a function of the data input line. The operating sequence starts with the availability of base current. When the data to be written into the memory is a "1" (high voltage on data input line), the upper inverter stage I1 will turn on. The output of I1 is connected externally to I2 to keep I2 turned off. The output of I1 is now near ground level and can sink base current from the output transistor Q1. If a write operation is to be executed the write timing generator will supply a positive 5V pulse to the emitters of the output transistors Q1 and Q2. Transistor Q1 will turn on, due to the base current path provided by the conducting inverter stage I1. Collector current in transistor Q1 flows through the D switch in a direction to write a "1" into the memory. Conversely, if the data to be written into the memory is "0" (low voltage level on data input line), the lower inverter stage I2 will turn on and make base current available to output transistor Q2. In coincidence with the write timing generator pulse, collector current will flow in the transistor Q2 to cause a "0" to be written into the memory.

Design Details

The two input inverter stages, being part of a monolithic integrated circuit, have operating limits specified and guaranteed by the manufacturer. In this application the units operate far below the specified limits to insure reliable performance.

The output stages are designed to supply 7 ma minimum and, under some conditions, 15 ma maximum current into the D switch. The 7 ma minimum current is based on the worst case condition for the D switch; the worst case condition for the digit driver will exist at a possible D switch requirement of 11 ma at -10° C. This can occur when semiconductor voltage drops are at their lower limits while the power supply is high. The worst case base current required to drive the output transistor Q1 or Q2 is 220 ma. The minimum base current available to the output transistors is 370 ma which is equivalent to a beta of 30.

The output transistors Q1 and Q2 have a minimum saturated end of life beta of 40 at -10° C.

Breadboard Module Evaluation

The Digit Driver circuit was assembled and tested at all combinations of voltage and temperatures with the following observation:

Output of Q1 or Q2:

Worst case delay:	8 nanoseconds at -10° C measured from write timing generator
Worst case rise time:	30 nanoseconds at -10° C
Worst case fall time:	50 nanoseconds at +85° C

Parts Specifications

Part	Value (ohms)	Breadboard	Prototype
R1,	3,000	RC07GF302J	RC05GF302J
R2,	3,000	RC07GF302J	RC05GF302J
R3,	6,800	RC07GF682J	RC05GF682J
R4,	6,800	RC07GF682J	RC05GF682J
R5,	100,000	RC07GF104J	RC05GF104J
R6,	100,000	RC07GF104J	RC05GF104J
Q1, Q2		2N3249	2N3249 in TO-46 can
Integrated Circuit		Signetics CS720J	Signetics CS720J

Note: Two of the four gates in the CS720J are used by the Read/Write control circuit, Section 3.8.4

3.5.4 Digit Current Sink

The digit current sink (figure 3.5-8) provides the digit current for the plated wire memory plane. The current amplitude is temperature compensated to match the requirements of the plated wire memory plane.

This circuit receives its input signal from the write timing generator.

During the Write operation, the output current pulse goes to the proper digit line of the memory system by way of the D switches and the digit selection matrix. During Read, this circuit remains inactive.

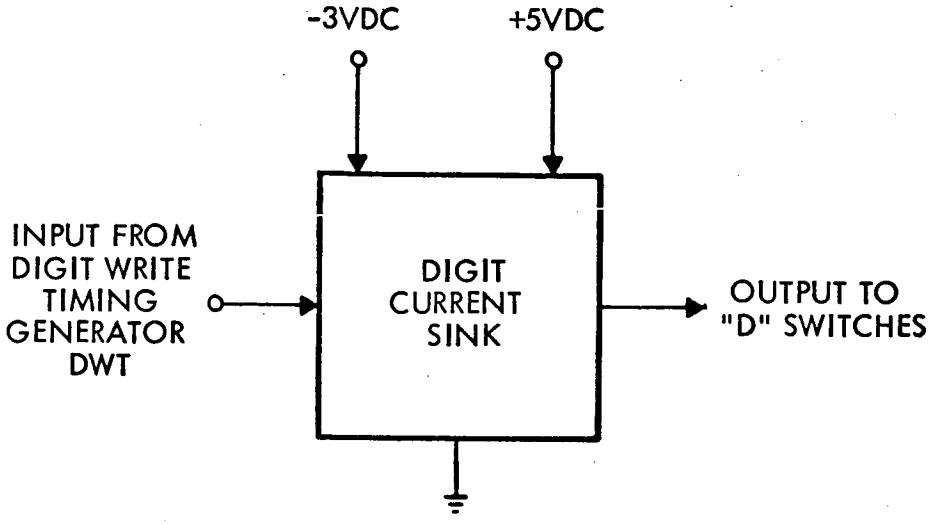

Figure 3.5-8. Digit Current Sink Elementary Diagram

Circuit Specifications

Conditions:

Operating temperature range: -10° C to +85° C
Nonoperating temperature range: -10° C to +139° C
Power input: -3 volts DC± 10% and +5 volts DC ± 10%
Signal input: A signal voltage within 0.5 volts of the +5 volt supply holds the circuit OFF. A level of 0 to +0.5 volt turns it ON.
Output load: 5 to 18 ohms referred to a voltage 0.7V less positive than the +5V power supply.
Duty cycle: 10% maximum

Performance: Power supply loading during the OFF period is limited to transistor leakage, which is negligible. A 100 kHz Write repetition rate with a duty cycle of 3 percent results in an average loading of 3.0 ma ±20% on the -3 volt supply and 0.25 ma ± 20% on the +5 volt supply.

Loading of the input circuit provides a temperature-compensated current sink for the digit line within the limits shown by the solid lines in figure 3.5-9. These limits are within ±7% of the nominal value of digit current required by the memory. The broken lines indicate ± 10% limits of digit current required by the plated wire memory plane specifications. The indicated performance will be attained for the breadboard load variation of 5 to 13 ohms, or, with a slightly different current level adjustment, the prototype load variation of 10 to 18 ohms. The output current pulse is within specification limits not later than 70 nanoseconds after the input waveform passes the 50 percent point.

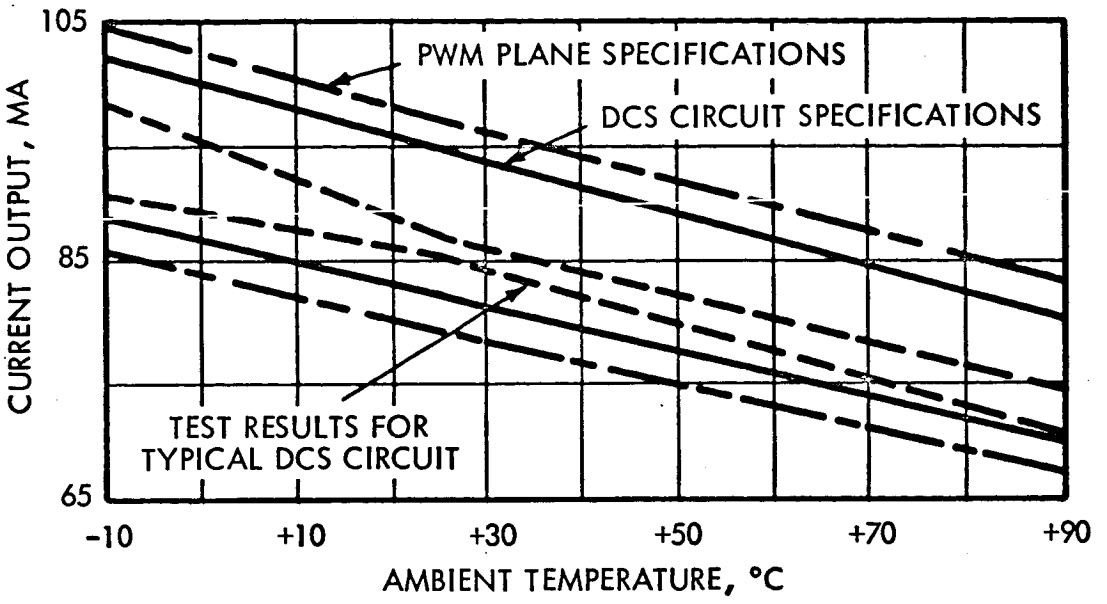

Figure 3.5-9. Digit Current Amplitude vs. Temperature

Circuit Description

As seen in figure 3.5-10, the circuit is inactive until the write timing generator supplies a pulse at the input terminal which pulls it down to 0.2V. This pulse turns on Q2 and the resulting voltage at Q2's collector drives current through R1. This current produces a stable voltage across the three series diodes CR1, CR2, and CR3. This voltage level, together with the resistance values of R3 and R4, sets Q1's collector current and therefore the output current to the proper level. Adjustments in output current level, to compensate for slight variations in characteristics of diodes CR1, CR2, CR3, transistor Q1, and the difference in loading between the breadboard and the prototype models, are made by changing the value of R4.

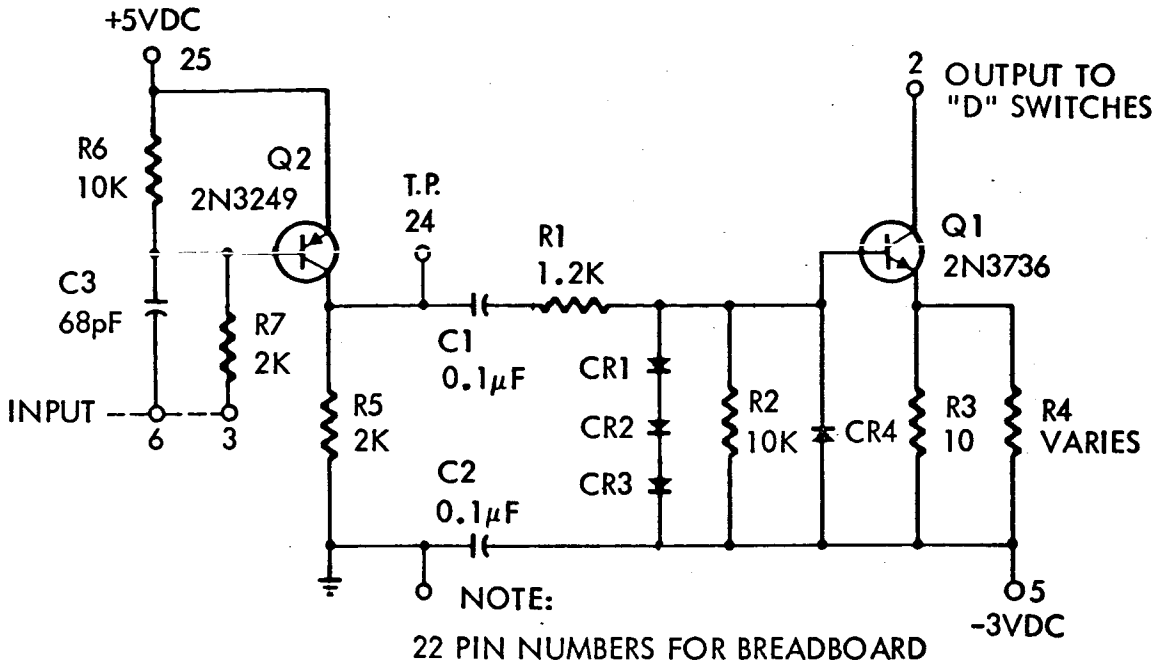

Figure 3.5-10. Digit Current Sink Schematic Diagram

Design Details

An input pulse level of 0 to 0.5 volts will cause a voltage drop of about 3 volts across R7, resulting in a base current of 1.5 ma. (See figure 3.5-10) This is sufficient to saturate Q2 and impress a minimum voltage of 4.0 volts across R5. This voltage pulse is coupled to R1 by blocking capacitor C1. The result is a current flow through R1 and into the three diodes CR1 through CR3.

During inactive period, C1 is charged to 3 volts through R5, R1, and CR4. Therefore, the voltage across R1 and CR1 through CR3 during a digit pulse will be approximately 4 volts. This drives the three diodes into a region where they act as a shunt voltage regulator, producing these results:

1. The proper voltage level to drive Q1 at 25° C
2. The proper voltage versus temperature characteristics to obtain the required output current curve.

Stability of the output digit current level is insured by using a metal film precision resistor for R3. Resistor R4 is provided as an adjustment for the nominal current at 25°C.

Breadboard Module Evaluation

The dotted curves of figure 3.5-9 show test results for an actual circuit. These limit curves reflect worst case combinations of power supply voltage variations for temperatures as shown. The load impedance was held constant.

Parts Specifications

Part	Breadboard	Prototype
R1, 1200 ohms	RC07GF122J	RC05GF122J
R2, 10K ohms	RC07GF103J	RC05GF103J
R3, 10 ohms	RN60D10R0F	RN50E10R0F
R4	Selected RC07GF	Selected RC05GF
R5, 2000 ohms	RC07GF202J	RC05GF202J
R6, 10K ohms	RC07GF103J	RC05GF103J
R7, 2000 ohms	RC07GF202J	RC05GF202J
CR1-CR4	Fairchild FD6331	Microsemiconductor MC9853
Q1	2N3736	2N3736
Q2	2N3249	2N3249 in TO-46 can
C1, C2	Sprague HY-320	Not Selected
C3	Sprague 5GA-Q68	U.S. Capacitor C10A680K

3.5.5 Read Amplifier (RA)

The requirement of the read amplifier (figure 3.5-11) is to detect a ONE signal coming from the plated digit wire and to convert this signal to a digital output with the desired characteristics. No output is required for a ZERO.

The read amplifier is a linear operating circuit which requires a continuous supply of power even during the absence of operating signals. In a read operation, the amplifier receives a signal from the plated wire

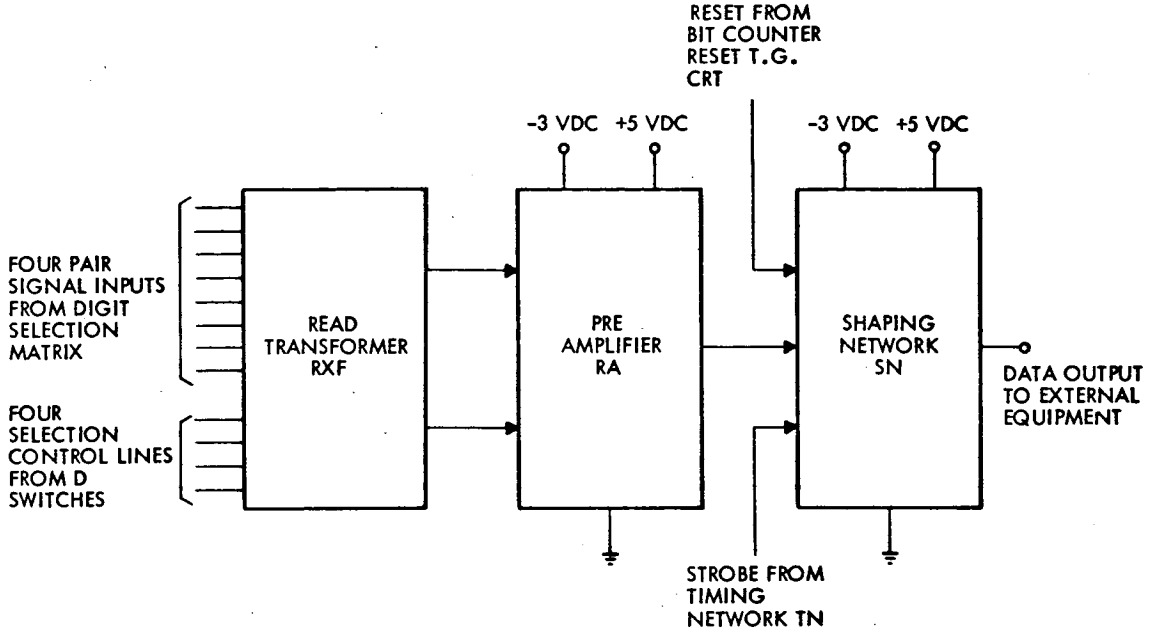

Figure 3.5-11. Read Amplifier Block Diagram

through a low impedance path through the digit selection matrix and read transformers. In a write operation, the amplifier is isolated from the digit matrix by reverse biased diodes in the read transformer modules.

In the breadboard unit the read amplifier is packaged in three separate modules: the read transformer modules RXF, the read reamplifier RA, and the shaping network SN.

The four individual read transformers now used represent a change from the original scheme, where one transformer with four primary windings was shown. Such a transformer was built and evaluated. The number of windings, their interconnection, and the required degree of balance

proved to be very critical, when incorporated in a single transformer. For the breadboard unit it was therefore decided to use four separate transformers.

Circuit Specifications

Conditions: This circuit will operate properly under the following conditions:

Temperature: operating: $-10^{\circ}C$ to $+85^{\circ}C$
non-operating: $-10^{\circ}C$ to $+139^{\circ}C$
Power Supply: +4.5 to +5.5 Volts, DC
-2.7 to -3.3 Volts, DC
Input for "1": positive polarity of 1.35 mv min.
for "0": negative polarity of 1.0 mv min.
Output: + 4 to +5 Volts at 4.0 ma max.

Performance

Power loading is continuous, +5 Volts: 3.5 ma
-3 Volts: 3.3 ma

During Read "1", the +5 Volt terminal will draw a maximum of 4.0 ma.

Circuit Description

The method of selecting a specific digit wire and connecting it to the read amplifier will be reviewed briefly with reference to the simplified selection diagram of figure 3.5-12.

The bit counter will place a +5 Volt level on the center taps of the set of four selection transformers in a vertical column of the digit selection matrix. For a Read operation, the selected D switch activates a read gate, thereby connecting a control input in the read transformer (pin 16 in figure 3.5-12) to near ground potential. Current now flows from a bit register flip-flop, through the primary windings of the selected digit matrix transformer and diodes, through the read transformer primary windings and diodes, and into the D switch. A voltage induced on the selected digit wire by a current pulse in a word line will find a low impedance path through the selected matrix transformer into the selected

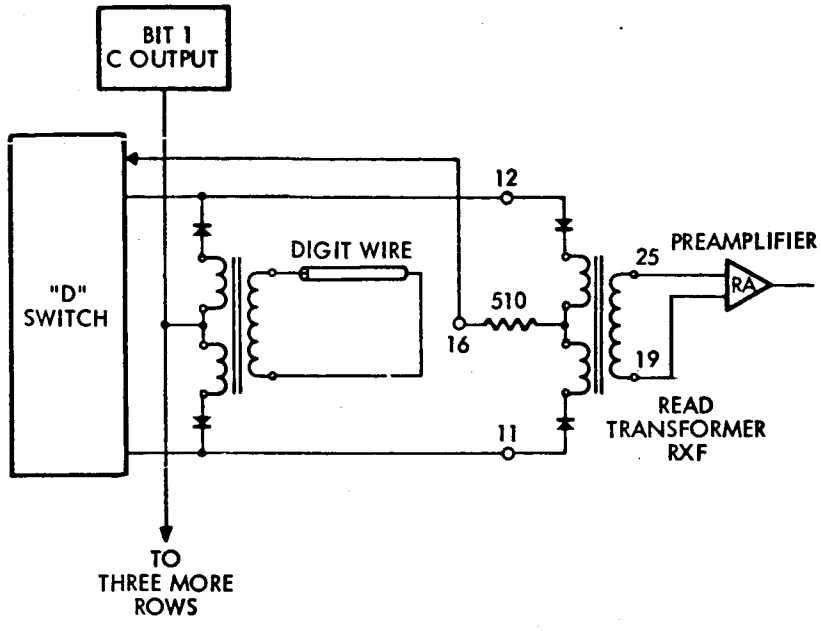

Figure 3.5-12. Simplified Read Signal Selection Diagram

read transformer and on into the read preamplifier. The complete read transformer module schematic is shown in figure 3.5-13.

A Fairchild 702A broad-band integrated amplifier is used as a preamplifier (figure 3.5-14) to obtain a minimum voltage gain of 60 at a bandwidth of nearly 10 mHz. This unit operates from low voltage supplies (+5V and -3V) with a total power drain of 25 mw.

The output of the 702A is not of sufficient amplitude to operate the output flip flop in the Shaping Nework (figure 3.5-15); for this reason two more amplification stages, Q1 and Q2, (figure 3.5-15) are used. These stages are biased for low conduction to minimize power drain. Another feature of this amplifier is the high ratio of gain during the time a readout

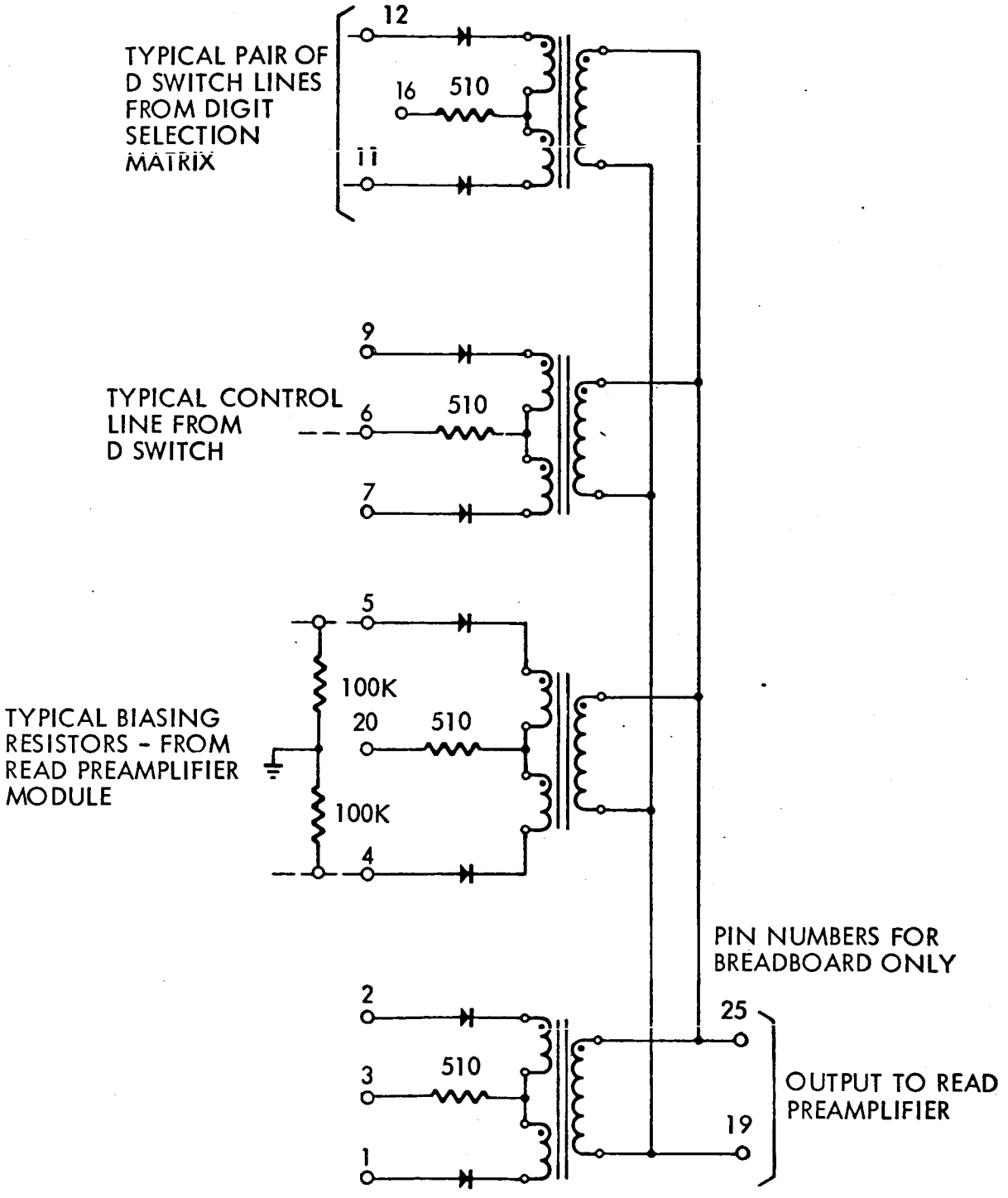

Figure 3.5-13. Read Transformer Schematic

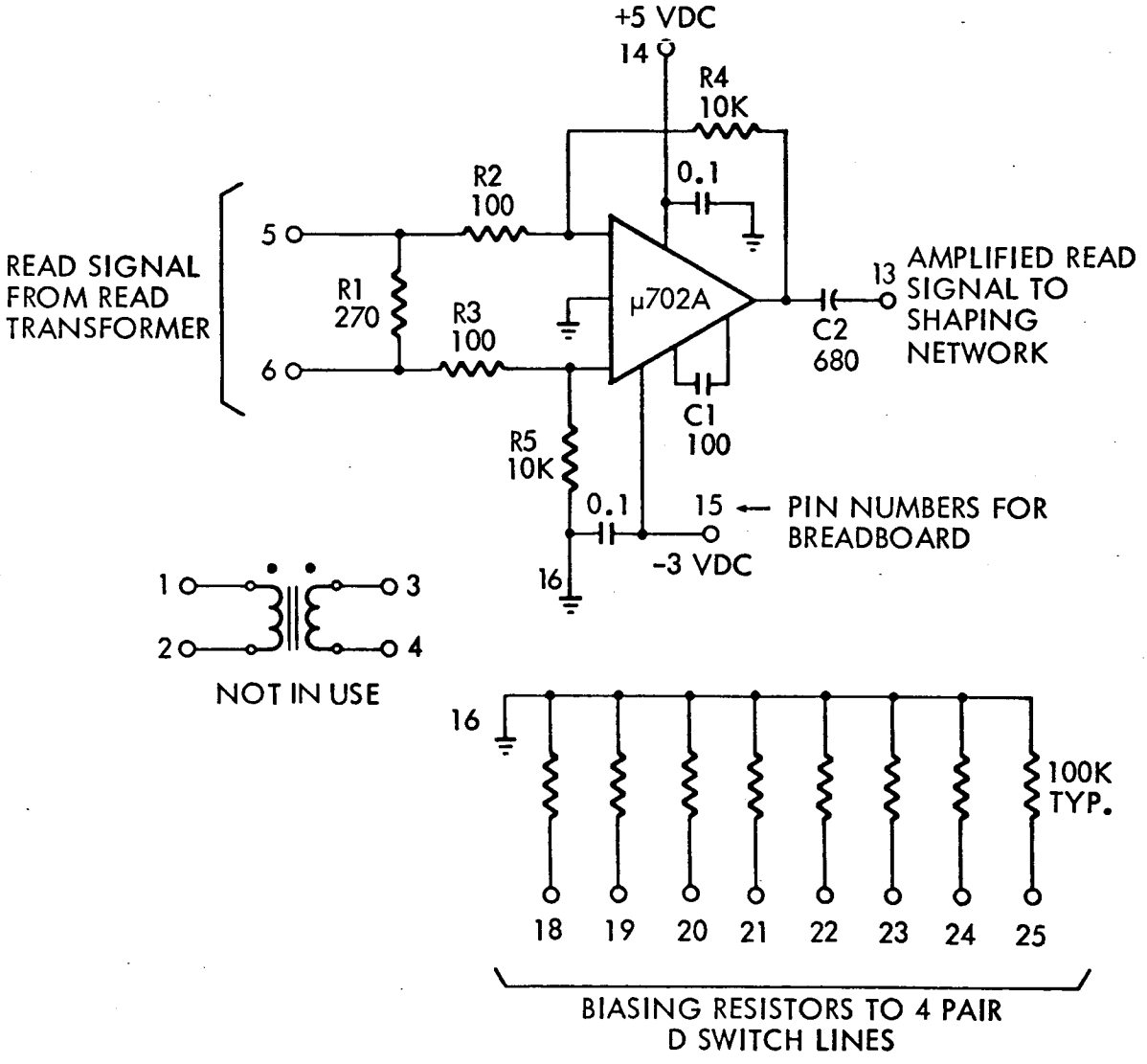

Figure 3.5-14. Read Amplifier

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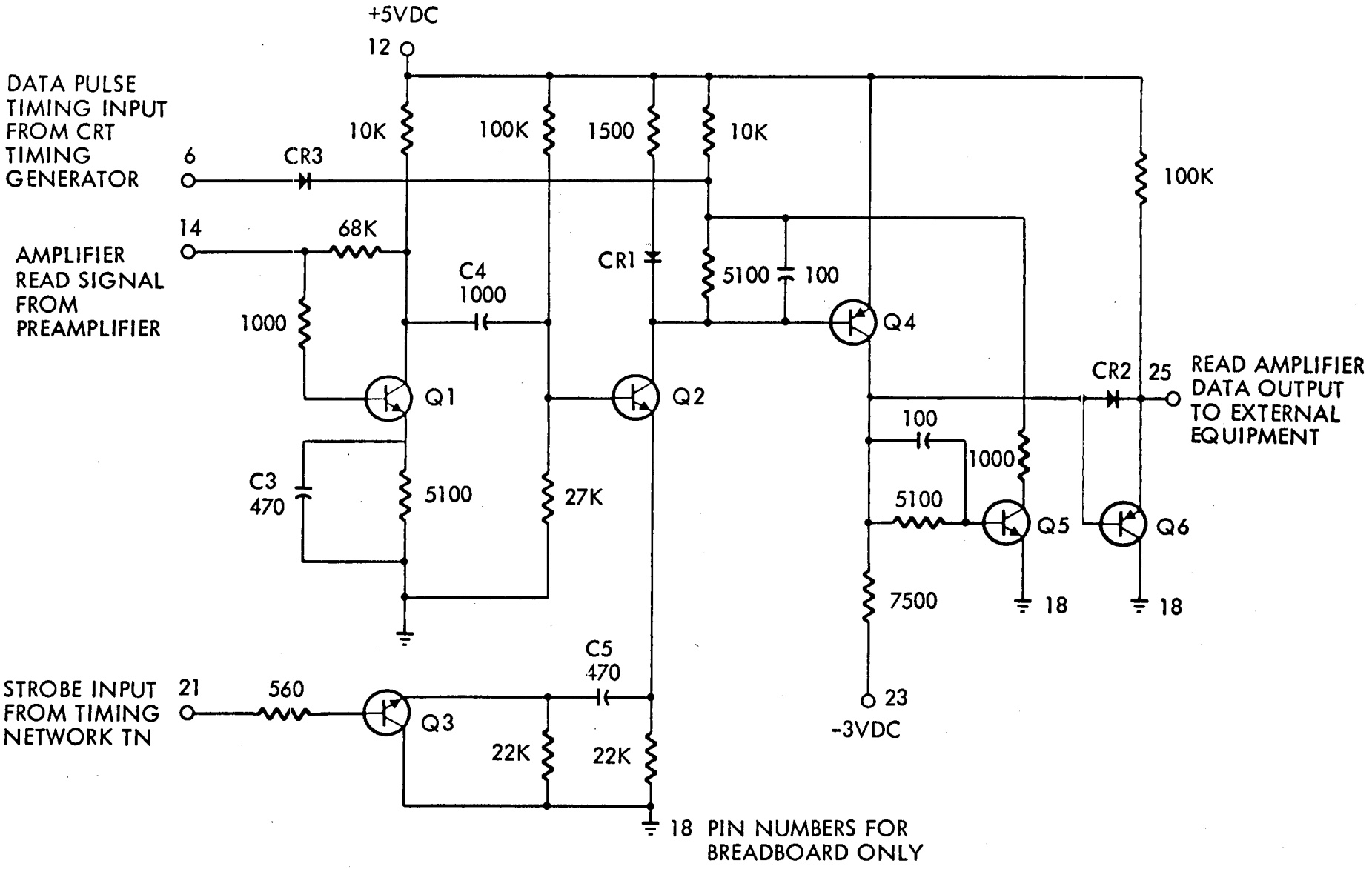

Figure 3.5-15. Read Amplifier Shaping Network Schematic

signal occurs to the gain at other times in the operating cycle. This variation in gain is controlled by Q3 which controls the emitter impedance of Q2. Normally, Q3 is not conducting. The impedance at the emitter of Q2 is approximately 11,000 ohms. With this much degeneration, the gain of Q2 is very low. In coincidence with a read signal coming from the pated digit wire, a strobe pulse is applied to the base of Q3. The transistor Q3 turns on to provide a low impedance path to ground for the emitter of Q2 and the gain is therefore increased.

A "1" signal will be negative in polarity at the base of Q1 and positive at the base of Q2. During the strobe, the collector of Q2 will go negative and turn on Q4. Transistors Q4 and Q5 form a flip-flop which remains on after the termination of the read signal.

Transistor Q6 is an output stage normally providing a low impedance zero signal level. When a "1" is read in the memory, the collector of Q4 puts a positive logic "1" voltage level on the output terminal through CR2. This voltage remains for one microsecond, at which time a positive going reset pulse at input pin 6 resets flip-flop Q4-Q5 and the output returns to ground level.

Design Details

No attempt has been made to obtain maximum gain from amplifier stages Q1 and Q2 in the shaping network (figure 3.5-15). Had it been done, this would have required high power in standby, which is undesirable in this system. The minimum gain required is that sufficient to guarantee that a minimum "1" signal at the input will set flip-flop Q4-Q5. A voltage change at the collector of Q2 of 900 millivolts is required to turn on the flip-flop.

The quiescent voltage at the base of Q4 with respect to its emitter is 300 millivolts minimum at high temperature. This voltage tracks the drop in diode CR1 over the operating temperature range, resulting in a uniform flip-flop triggering level.

The voltage gain of Q1 is low at the frequencies of concern here. This is due to the high collector impedance and high effective collector-to-base capacitance. The effective collector-to-base capacitance is the actual capacitance multiplied by the gain of this stage (Miller effect). The total voltage gain of the amplifier Q1 and Q2 is 9. A minimum "1" input (negative polarity at the base of Q1 of 100 millivolts is therefore required to set the flip-flop.

The integrated preamplifier 702A (figure 3.5-14) has a minimum open loop voltage gain of 300 at low temperatures and low operating voltages of +5 and -3 volts. The minimum closed loop voltage gain with feedback as used here is 74. A minimum "1" voltage (positive polarity) of 1.35 millivolts is therefore required at the input to the preamplifier, in order to generate an output in the shaping network. The actual output signal from the plated digit line will have to be slightly higher to compensate for losses in the transmission path.

The differential input impedance to the preamplifier module is 132 ohms. The transmission path consists of the line resistance plus two conducting diodes in each leg as shown in figure 3.5-16. The total resistance in each conducting leg is 22 ohms. Hence the output signal generated is 1.8 millivolts minimum, in the absence of noise. The "0" signal required is that necessary to overcome noise, so that the composite signal at the amplifier input is zero.

Parts Specifications

Part	Breadboard	Prototype
Preamplifier	Fairchild 702A	Fairchild 702A
Q1, Q2, Q3, Q5	2N2369A	2N2369A in TO-46 can
Q4, Q6	2N3249	2N3249 in TO-46 can
Diodes	Fairchild FD6331	Microsemiconductor MC9853
Resistors:	R2, R3 are matched .1%	RC05
	R4, R5 are matched .1%	RC05
	All other resistors are ±5%	RC05
Capacitors:	±10%	U.S. Cap. C-10 Series

Transformers are the same as those specified in Section 3.5.1.

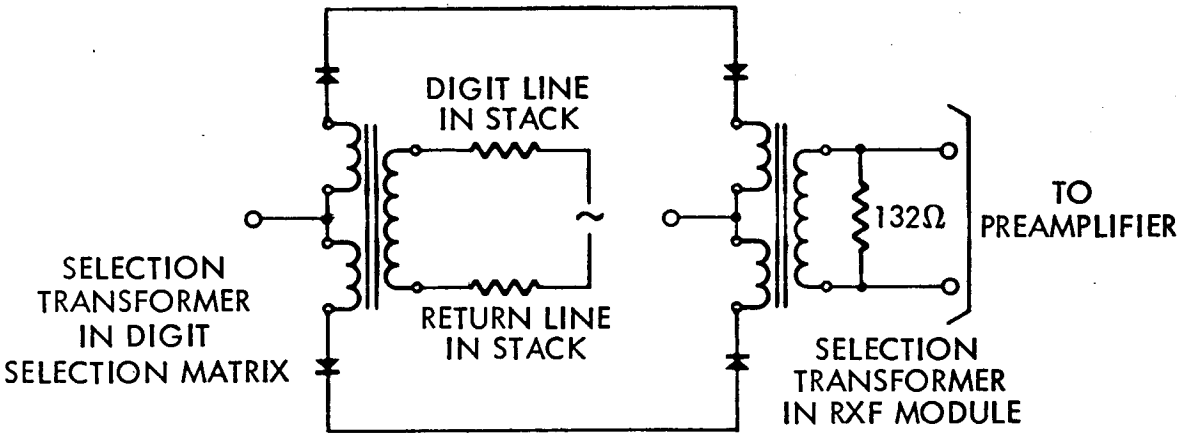

Figure 3.5-16. Basic Read Signal Path

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3.6 WORD ELECTRONICS

The word electronics (figure 3.6-1) selects and drives a shaped current pulse through one of 64 word lines in the breadboard memory stack (one of 256 for the prototype). Inputs to the word electronics are: Power from the +15 volt bus; power from the Voltage Regulator Switch; address information; and timing from the timing network. The word electronics is active for both a Read and a Write operation.

Circuit Specifications

See Specifications for individual circuits

Circuit Description (figure 3.6-2)

With all input signals off, all word electronics circuitry will be off. The memory stack lines B1 through B8 will be held at +15 volts by biasing resistors RB1 through RB8; lines A1 through A8 will be held at ground by resistors RA1 through RA8.

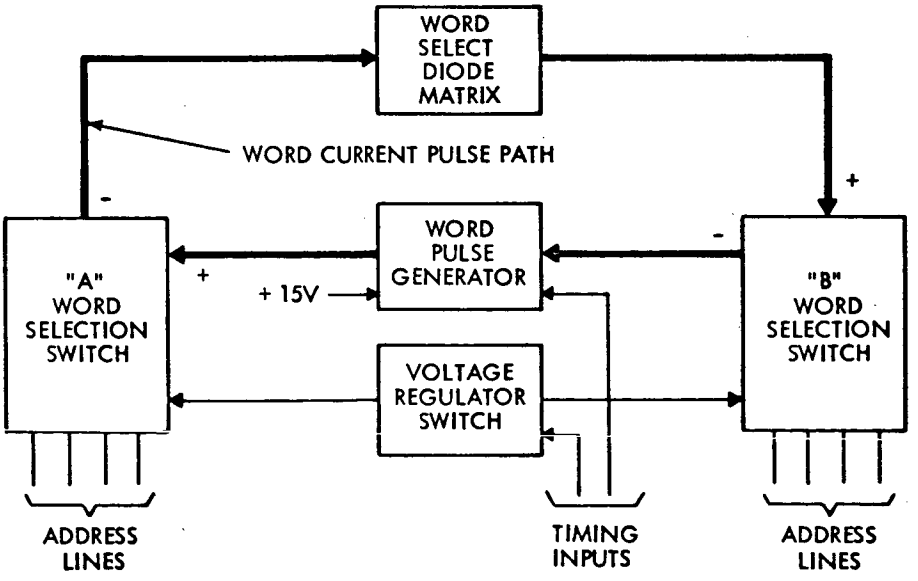

Figure 3.6-1. Word Electronics Block Diagram

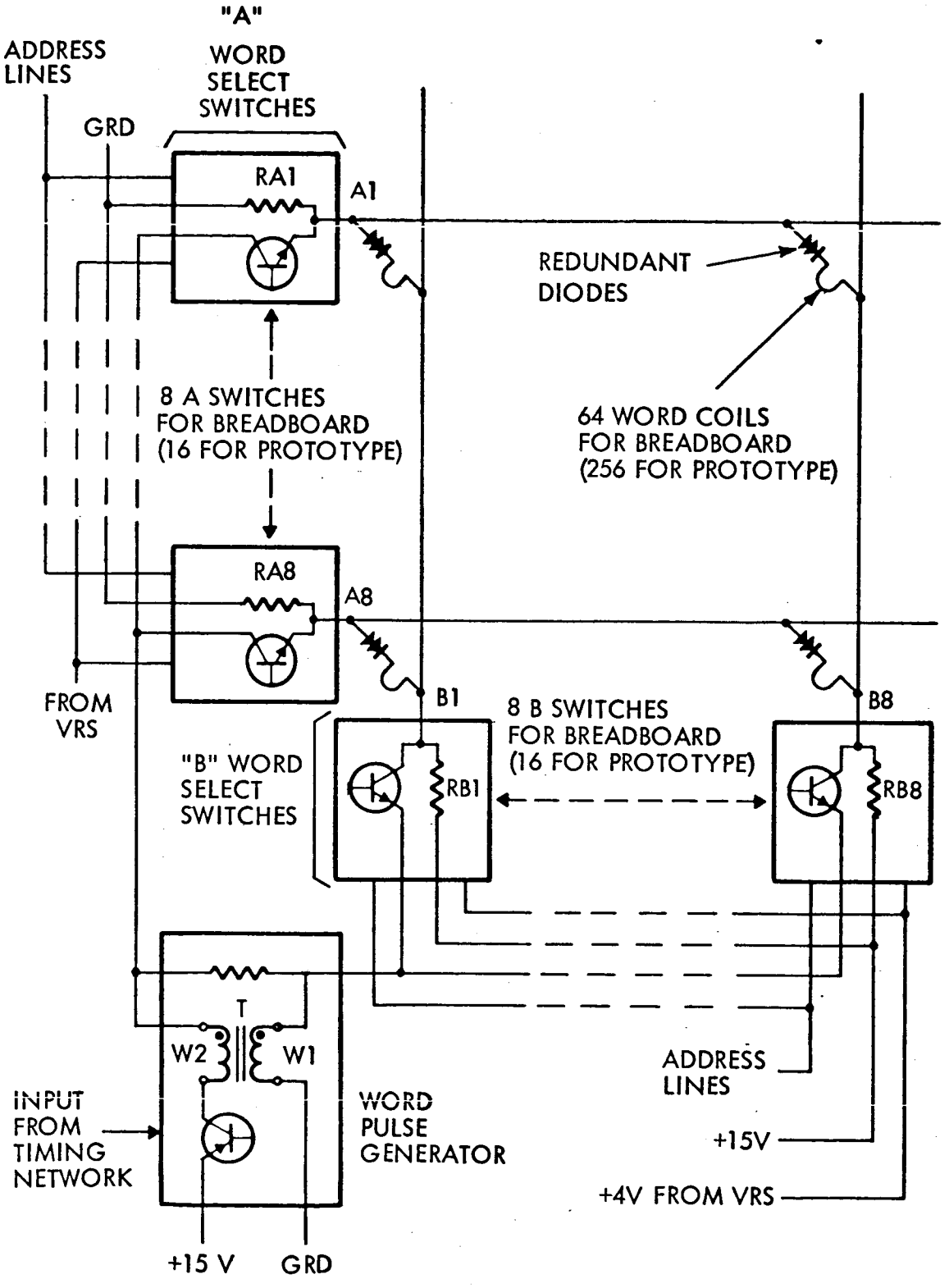

Figure 3.6-2. Word Electronics Simplified Schematic

Immediately prior to and during any memory operation the address lines will be stable. Upon receipt of a command to execute a READ or WRITE operation the timing system will turn on the Voltage Regulator Switch for one microsecond. This will turn on one of the 8 "A" and one of the 8 "B" word select switches with the selection determined by the states of the address lines.

When a "B" word switch turns on, it discharges its output line to the memory stack to ground through common mode choke T in the word pulse generator. Since winding 2 (W2) of the choke T is essentially open (word pulse generator is "off"), the charge on the selected B line in the memory stack will be removed at a rate dependent upon the capacity of the B line and the inductance of winding 1 (W1) of choke T. The inductance of choke T is set so the B line capacity will be discharged to ground in approximately 500 nsec. At this time, both the selected A and B lines will be at ground potential. When the word pulse generator is turned on, current can pass only through the selected A and B switches and through the unique diode and word line connected to the selected A and B lines. Any one of the 64 (256) word lines in the stack may be selected by properly specifying the states of the address lines.

When the memory operation is over and the voltage regulator switch and the word pulse generator are de-energized, the Resistor RB associated with the previously selected B line will charge that line and its associated capacity to +15 volts in less time than the minimum interval between memory operations.

Two diodes in series per word coil are used in the memory stack. Series redundancy of the diodes greatly reduces the probability that diode malfunctions in one word line will deleteriously affect the whole stack.

3.6.1 Refer to Section 3.6, the description of the complete word electronics circuits, for a description of the word selection matrix.

The matrix for the breadboard stack uses two diodes, Microsemiconductor MC9853, in series per word coil. The prototype memory will use a

dual diode, MC9962, instead. The latter consists of two diodes welded in series connection by the diode manufacturer.

The word selection matrix is packaged on the memory modules in order to minimize radiation, wire lengths, and connection count. On the prototype memory stack, 256 pair of word coil terminals are matrixed so that only 32 wires are needed to connect the rest of the word electronics into the stack.

3.6.2 A and B Word Selection Switches

There are 16 word selection switches (figure 3.6-3) in the breadboard memory and 32 in the prototype. These switches are identical and interchangeable. They perform the function of decoding the input address information and enabling a current path through the desired word line in the memory stack.

Each selection switch is driven by a unique combination of four address lines. Power is applied to the circuit via the voltage regulator switch.

The selection switch acts to close a current path between the word pulse generator and the diode-isolated word matrix in the memory stack.

For any memory operation, two of the 16 (or 32) selection switches are energized. The selection is determined by the states of the input address lines.

Power consumption of these circuits is zero while the memory is in standby. When the memory is in operation, power is applied through the voltage regulator switch for one microsecond duration at each clock pulse, thus minimizing the average power drain of the system.

The two switch output leads have no conductive path to ground (or to any power supply) regardless of whether the switch is "ON" or "OFF". This allows a flexibility in application similar to that provided by a relay contact.

The A and B switches are identical in construction. They differ in application only.

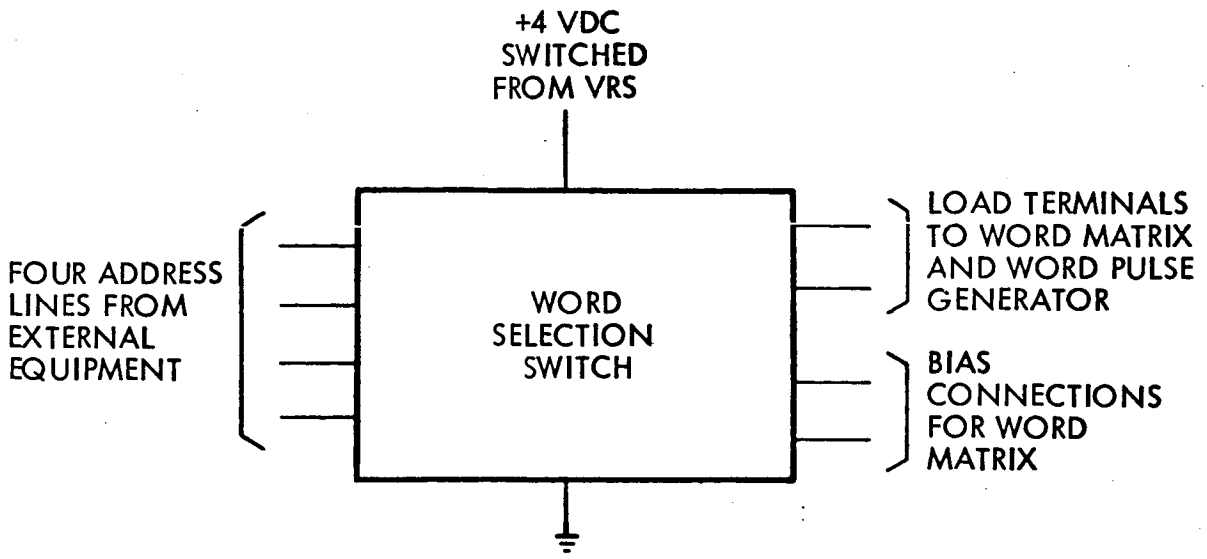

Figure 3.6-3. A and B Word Selection Switch Elementary Diagram

Circuit Specifications

Conditions:

Ambient Temperature, operating: -10°C to +85°C
non-operating: -10°C to +139°C
Input address signal voltage, 1 condition: +2.5V to +6.0V
Input address signal voltage, 0 condition: 0V to +0.7V
Switched power: -10°C, +4.3V, ±0.2V
+25°C, +3.9V, ±0.1V
+85°C, +3.3V, ±0.2V
Output current: 242 ma maximum
Maximum duration of output pulse: 800 nanoseconds

Performance:

This circuit performs within limits specified below for all combinations of applied conditions specified above.

Power supply loading, off condition: 1 ma maximum
Power supply loading, on condition: 32 ma ± 25%

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Address input load, "1" condition: 25 microamperes maximum into each selection switch input.

Address input load, "0" condition: 0.9 ma maximum from each switch is divided among its "0" signal inputs.

Address input load for 16 (32) switches: A total of 14.4 (28.8) ma maximum is supplied to the set of 6 (8) address lines which are at "0" level. Division of load is unequal to the extent that the signal sources have unequal characteristics. The sources having better "0" levels tend to take more than their share of the load.

Output saturation voltage (on): 1 Volt maximum.

Output "off" current: transistor leakage only.

Turn-on Time: the output transistor will reach "on" saturation within 100 nsec. or less from the time the input power supply voltage reaches 80% of steady state "on" amplitude.

Turn-off Time: the output transistor will reach "off" saturation within 50 nsec or less from the time the input power supply voltage falls below 10% amplitude.

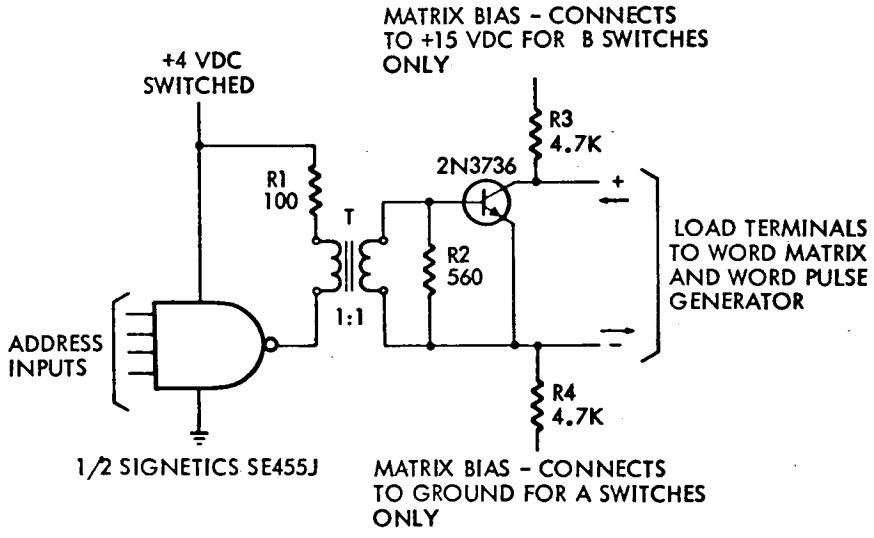

Figure 3.6-4. A and B Word Selection Switches Schematic

Circuit Description

The word selection switch (Figure 3.6-4) consists of an integrated-circuit four-input AND gate driving a transistor switch. Two identical word selection switches are packaged in each circuit module.

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Normally, the power from the voltage regulator switch is off and no power is dissipated in the switch circuit. The voltage regulator switch timing is such that the address input lines are at a steady state "1" or "0" during the time the voltage regulator switch is ON. If any of the address input lines to the word selection switch are in the "0" state (0 volts) the integrated AND gate will not turn on with the application of power from the voltage regulator switch. However, if all address input lines are in the "1" state (+5 V) the integrated AND gate will turn on and the output will sink current from the voltage regulator switch through resistor R1 and transformer T.

In turning on, the integrated AND gate will force base current to flow into output transistor Q1, driving it to saturation. The base current supplied to Q1 is sufficient to keep it in saturation for the entire interval in which the voltage regulator switch is applying power to the circuit.

When the voltage regulator switch turns off, removing power from the circuit, the inductance of transformer T will cause the base-emitter junction of Q1 to be back biased, resulting in rapid turn off. Resistor R2 limits the reverse voltage applied to the base of Q1 to a safe value.

Resistors R3 and R4 are biasing resistors for the diode matrix in the memory stack. When the circuit is used as an "A" switch, R4 is connected to ground and R3 is left unconnected. When the circuit is used as a "B" switch, R3 is connected to +15 Volts and R4 is left unconnected. Both resistors are included in each switch circuit to provide interchangeability.

The integrated circuit used is the Signetics SE455J low power four-input buffer-driver. Each flat pack contains two identical gates, one of which is shown in figure 3.6-5. Operation is as follows:

Case 1: one or more inputs in "0" (ground) state. When power is applied to the circuit by the voltage regulator switch the input line(s) in

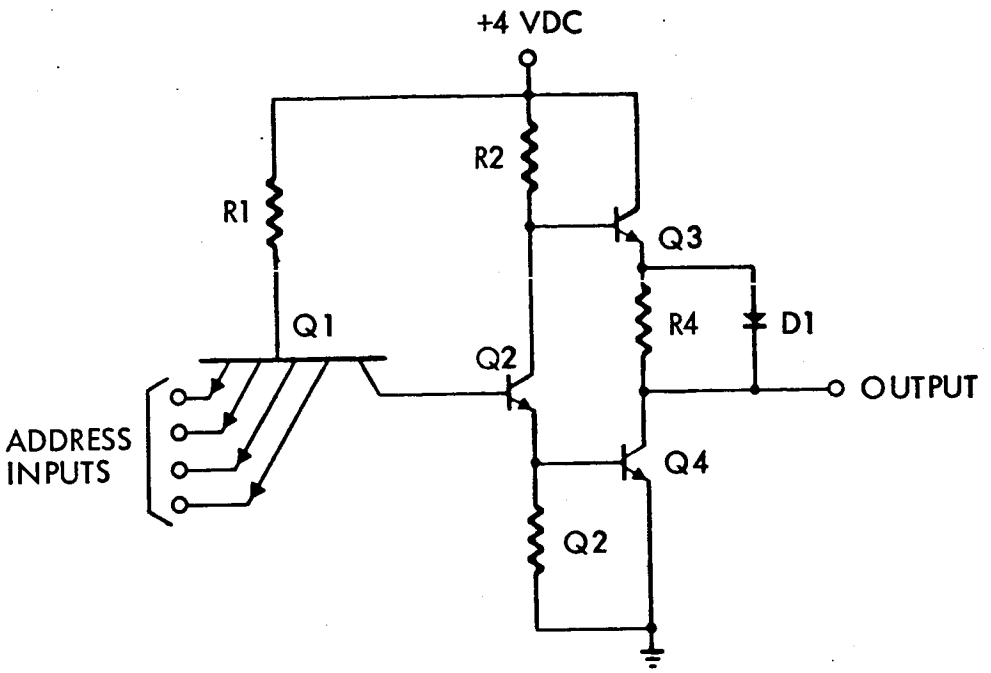


Figure 3.6-5. Signetics SE455J Gate Schematic

the "0" (ground) state will sink the current from R1 through the forward biased base emitter junction(s) of Q1. No current will be available to turn Q2 on so that Q2 and Q4 will remain off. The output line will be pulled positive through D1, R4, and Q3.

Case 2: all input lines in "1" (+5V) state. When power is now applied to the circuit by the voltage regulator switch the current through R1 will forward bias the collector base junction of Q1 and turn on Q2. Current through Q2 will turn on Q4 which will pull the output to ground. Q2 being on also will sink the current through R2 keeping Q3 off.

The complete schematic for a breadboard word switch module is shown in figure 3.6-6.

Design Details

Maximum load current at -10° is 242 ma. Output transitor Q1 (figure 3.6-6) has a minimum end of life, low temperature beta of 20 for a

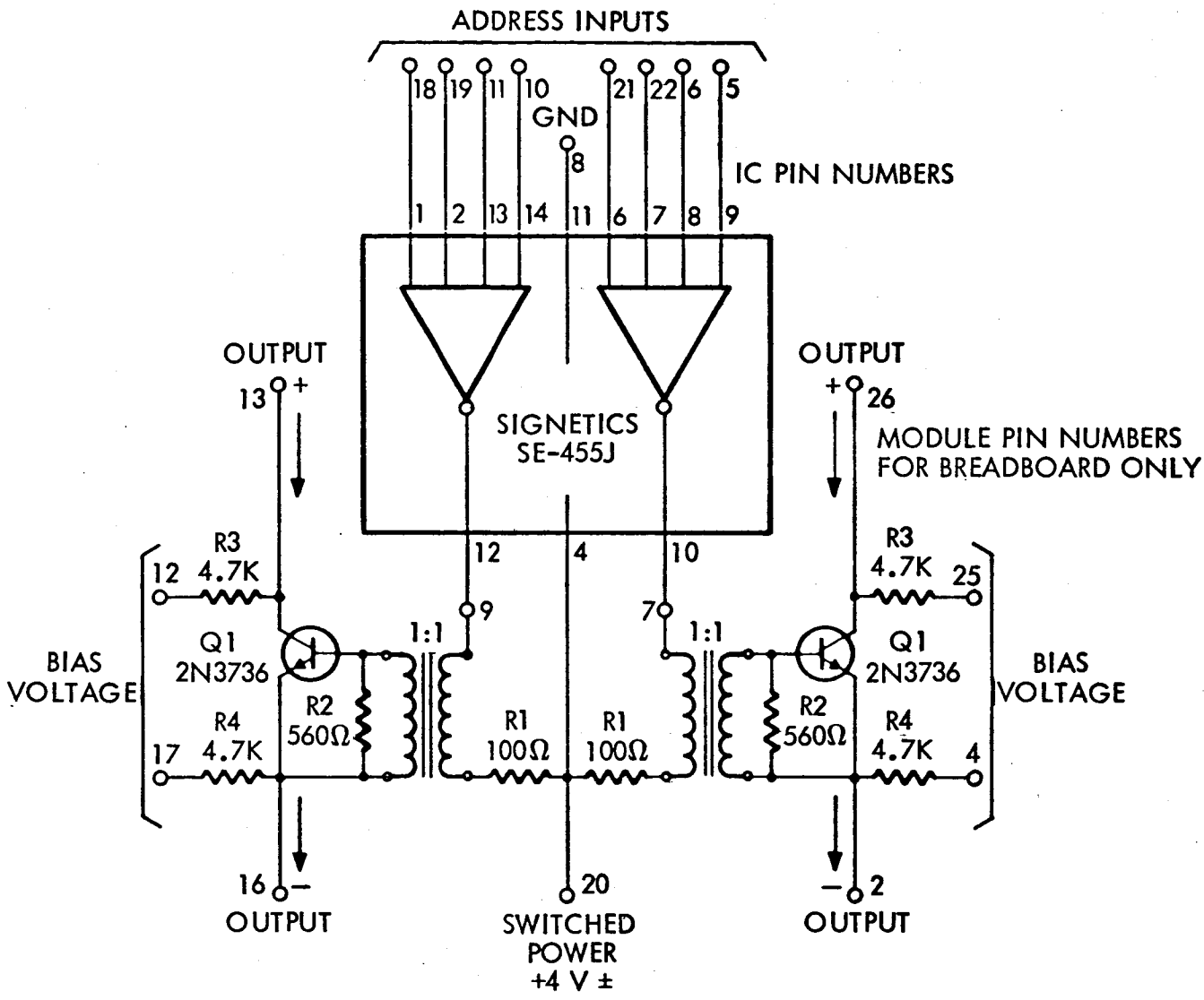


Figure 3.6-6. Dual Word Switch Module Schematic

collector current of 250 ma and a collector voltage of 1V. Q1 must have a minimum of 12.1 ma of base current. Another 2 ma will be taken by the 560 ohm damping resistor. Ten ma of magnetizing current is required by the 1:1 transformer (110 microhenries minimum inductance) by the end of the one microsecond "ON" interval. Therefore, the required drive to the transformer is 24.1 ma. The limiting resistor R1 is selected to make available the minimum required drive for the worst

operating conditions. The minimum total which the integrated gate is required to sink is 24.1 ma. The voltage output versus temperature characteristic of the voltage regulator switch complements the current drive versus temperature characteristic of the word select switch in that, as temperature decreases, the increased drive current required by the word switch is provided by the increased voltage output of the regulator switch. If the worst integrated gate is required to sink more than 27 milliamperes under worst case conditions the gate output may come out of saturation. This is inconsequential, however, because it will in all cases be able to pass more current than the minimum required.

Breadboard Module Evaluation

The word selection switch circuit used in the breadboard was tested at all voltage and temperature extremes with proper operation in all cases.

Observed data:

Turn on delay	100 nanoseconds
Turn off delay	50 nanoseconds

Parts Specifications

Part	Breadboard	Prototype
R1, 100 ohms	RC07GF101J	RC05GF101J
R2, 560	RC07GF561J	RC05GF561J
R3, R4, 4700	RC07GF472J	RC05GF472J
Transformer	Technitrol	Pulse Engineering "Flat Tran"
Q1	2N3736	2N3736
Integrated Circuit	Signetics SE455J	Signetics SE455J

3.6.3 Word Pulse Generator (WPG)

INTRODUCTION

The word pulse generator (figure 3.6-7) provides a shaped temperature-compensated current pulse to the selected word line in the memory for both a read and a write operation.

The WPG is controlled and timed by the timing network. The current pulse output passes through the selected A and B word select switches to the selected word line.

Circuit Specifications

Conditions:

Ambient temperature, operating: -10° to +85°C
non-operating: -10°C to +139°C
Power supply voltage: +13.5 to +16.5 volts DC
Input signal voltage, "on" condition: +2.0 to +6.0V
Input signal voltage, "off" conditions: 0 to +0.5V
Input signal voltage rise time: 0 to 50 nsec
Maximum duty cycle: 0.09
Capacity of load: 100 pf maximum

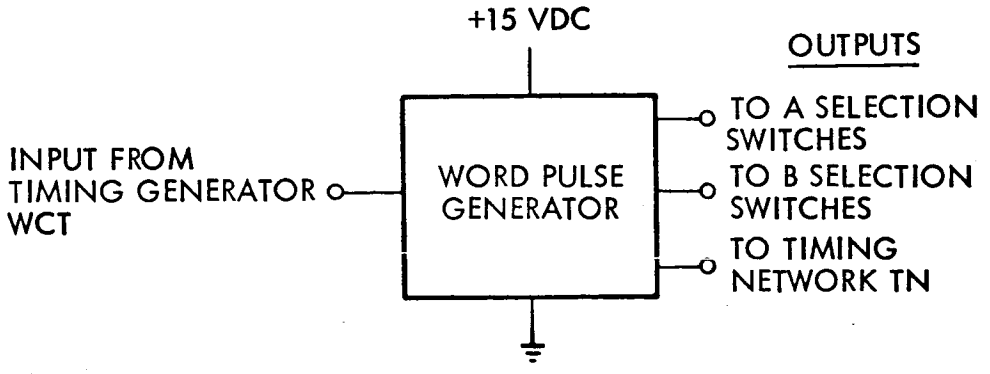


Figure 3.6-7. Word Pulse Generator Elementary Diagram

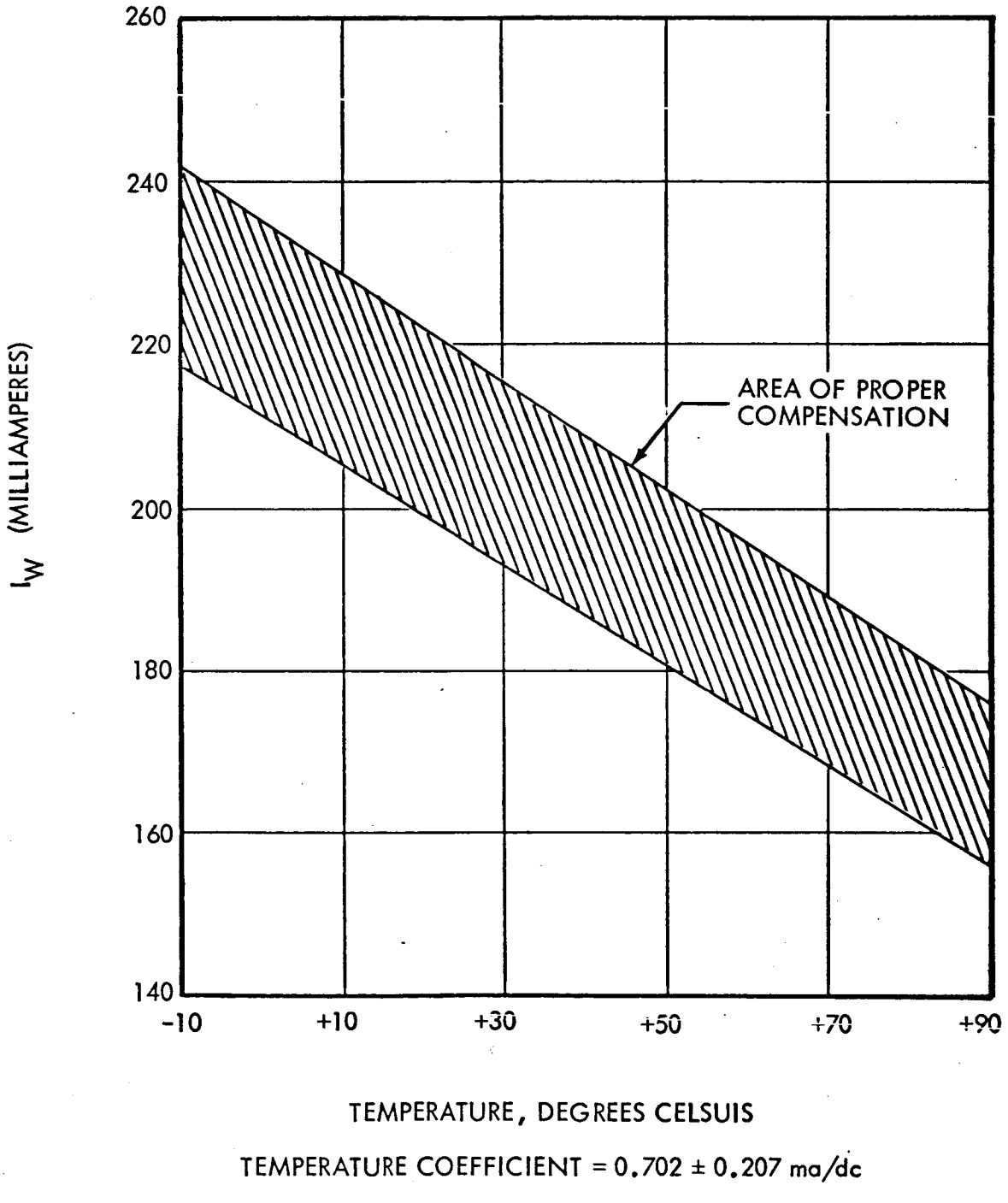


Figure 3.6-8. Word Current Requirements for Memory Planes

Performance:

The WPG will draw a maximum average current of 7.65 ma from the +15 volt power bus at maximum repetition rate.
The WPG requires a minimum of 1.0 ma input drive and a maximum of 5.65 ma.
The WPG will sink 0.135 ma maximum from the input line when input voltage is "off".
Output current as required by the memory planes is shown in figure 3.6-8.

Maximum current rise time (10% to 90%) into word line: 50 nsec
Maximum current fall time (90% to 10%) into word line: 60 nsec
Maximum current pulse delay: 50 nsec (measured from 50% point on voltage input to 50% on current output)

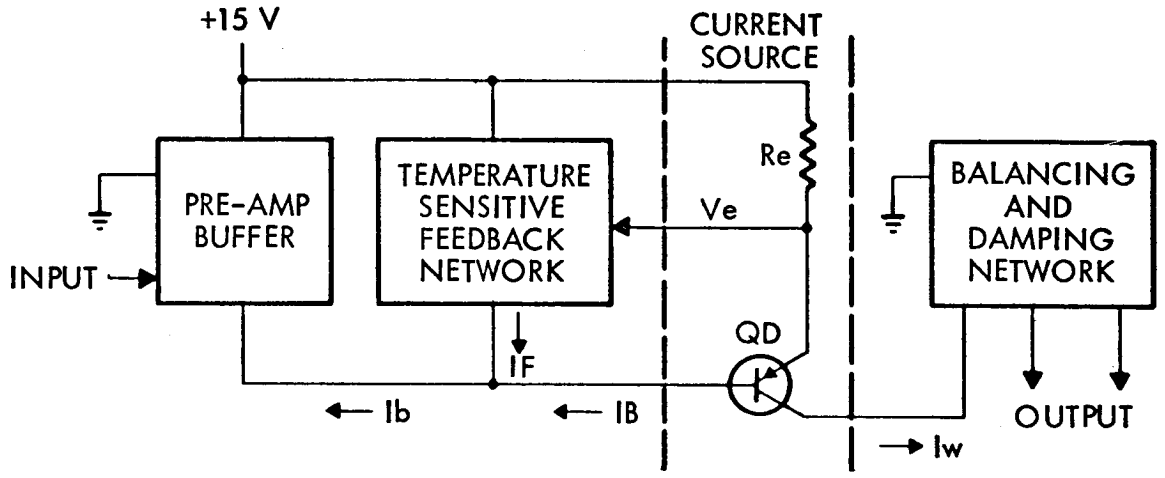


Figure 3.6-9. Word Pulse Generator Block Diagram

Circuit Description

The word pulse generator (figure 3.6-9) is composed of four parts: a pre-amplifier/buffer; a transistor current source; a feedback mechanism; and a balancing network.

When the input voltage is in the "off" condition, the pre-amp/buffer provides a reference to +15V for the base of QD, keeping QD off. When

the input changes to an "on" condition, the pre-amp/abuffer will sink a current, Ib, from the base of QD, which is much greater than the base current necessary to produce the word current pulse Iw. This overdrive results in a fast current pulse rise time. When Iw has risen to the value which is correct for the ambient temperature, Ve will be at some particular value. The temperature sensitive feedback network samples Ve and at the correct potential will supply current to the pre-amp/buffer in parallel with the base of QD. The amount of current supplied will be that amount which will leave the base current of QD at exactly that value required to maintain Iw at its correct value.

The balancing and damping network converts Iw to a sink and a source output, transiently balanced to ground. The output is also resistively damped.

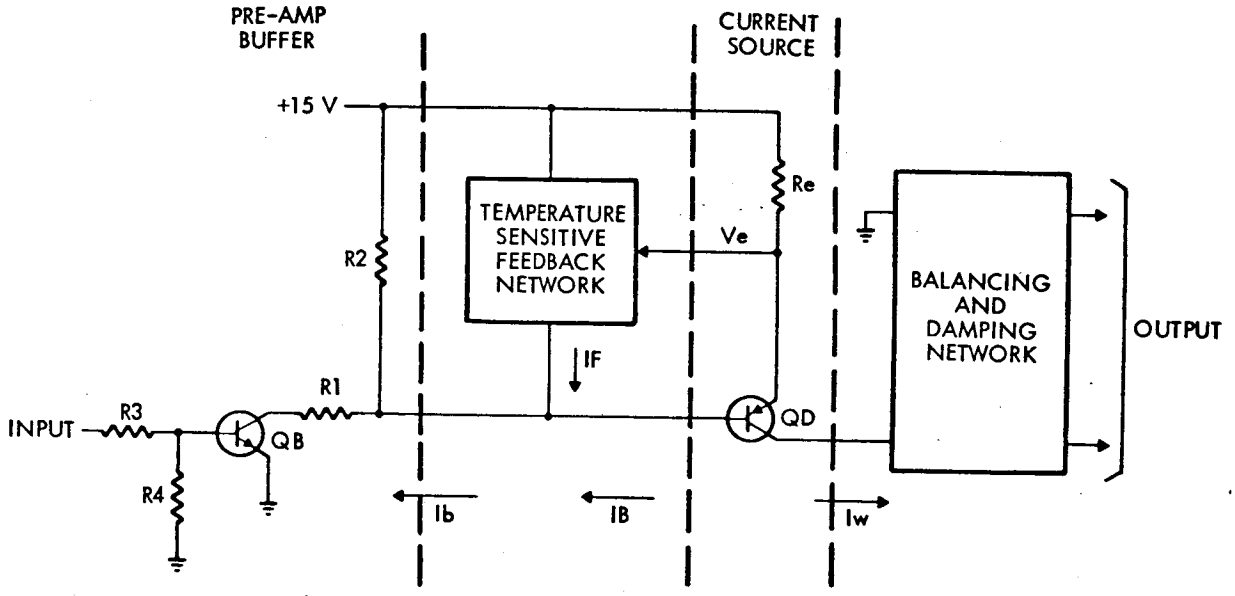


Figure 3.6-10. Preamplifier Buffer

The pre-amplifier/buffer circuit (figure 3.6-10) converts the logical input signal (off, 0V; on, +4V) to proper driving levels. When the input is "off," QB is off and the base of QD is referenced to +15V by R2, which is low enough in value to assure that QD is off. When the input is "on" (+4V), QB is on and R1 sinks the current necessary to drive QD.

R3 limits the maximum current into the base of QB while R3 and R4 together establish a QB turn-on threshold higher than the worst case "off" input potential.

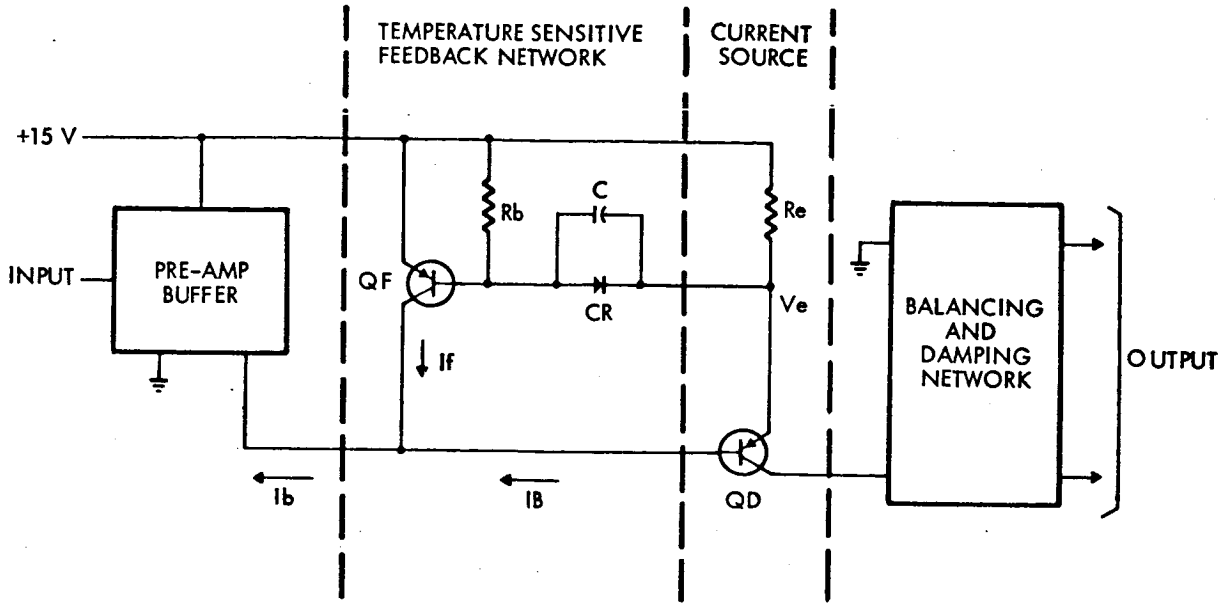


Figure 3.6-11. Temperature Sensitive Feedback Network

The temperature-sensitive feedback network (figure 3.6-11) regulates the output current, Iw, to that amount required at the ambient temperature of the system.

When QD is turned on by the pre-amp/buffer circuit, the current through QD (Iw) will result in a voltage drop, Ve, across Re. When the current has increased such that Ve minus the voltage drop across the diode, CR, causes QF to turn on and reduce the base current, Ib, driving QD. As Iw increases, If will increase, until a point is reached such that Ib is exactly equal to that current necessary to sustain Iw:

$$Ib = \frac{Iw}{\beta_{QD}}$$

The voltage, Ve, at which the circuit will stabilize is equal to the voltage drop across CR and that base-emitter voltage of QF which causes the

correct amount of feedback current, IF, to flow. The transconductance of QF varies with temperature as does the voltage drop across CR. The temperature dependence of CR is a function of the current through CR; by varying Rb, the temperature coefficient of the entire circuit can be varied to that required by the memory stack.

The output of the word pulse generator looks at a load consisting of the inductance of the word coil shunted by wiring capacitance. A damping resistor is provided in the balancing/damping network. It is purposely set larger than the resistance for optimum damping, as optimum damping would drastically increase the rise time of the current pulse through the word coil. The word pulse generator current output is tailored by the addition of the capacitor, C, shunting CR. The capacitor causes the output current waveform to have a "notch" on the rise time which approximately cancels the effect of the oscillatory current spike caused by the load capacitance. The result is a more perfectly trapezoidal current pulse through the selected word coil.

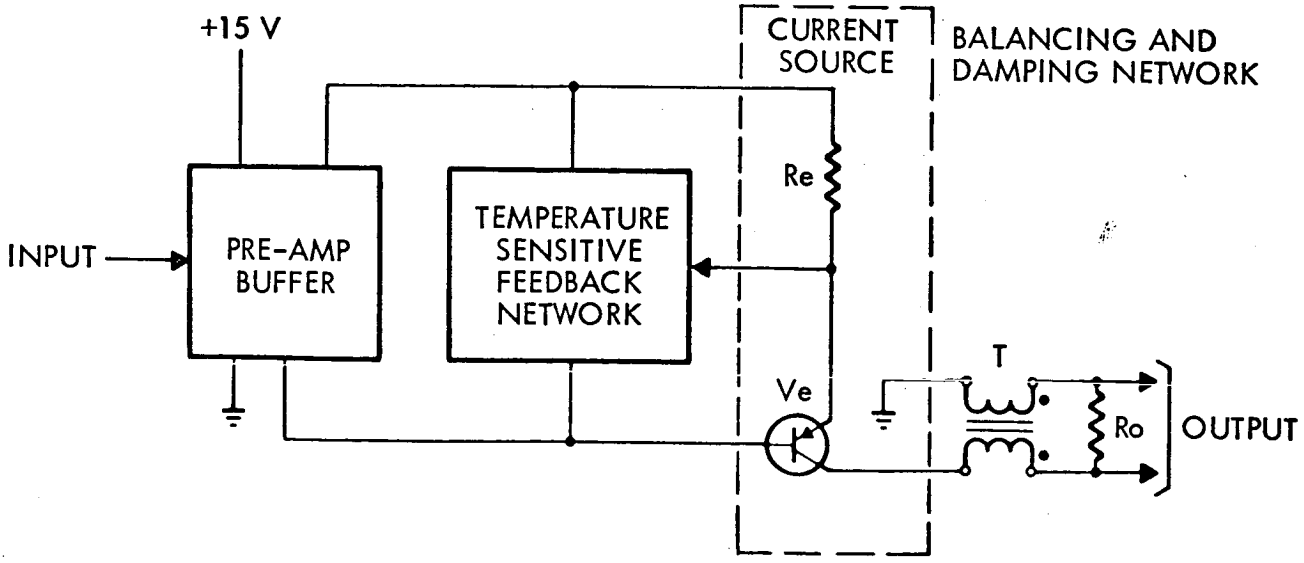


Figure 3.6-12. Balancing and Damping Network

The balancing and damping network (figure 3.6-12) converts the single ended output of the current source to a transiently balanced double ended output to the word select switches and selected word coil. This balanced drive results in a reduction of word line to digit line noise caused by the word current pulse. The damping resistor helps shape the word current pulse output by making the load look less reactive.

The complete schematic of the word pulse generator is shown in figure 3.6-13. In addition to the main outputs, a timing output is provided for the Timing Network which generates the read strobe pulse.

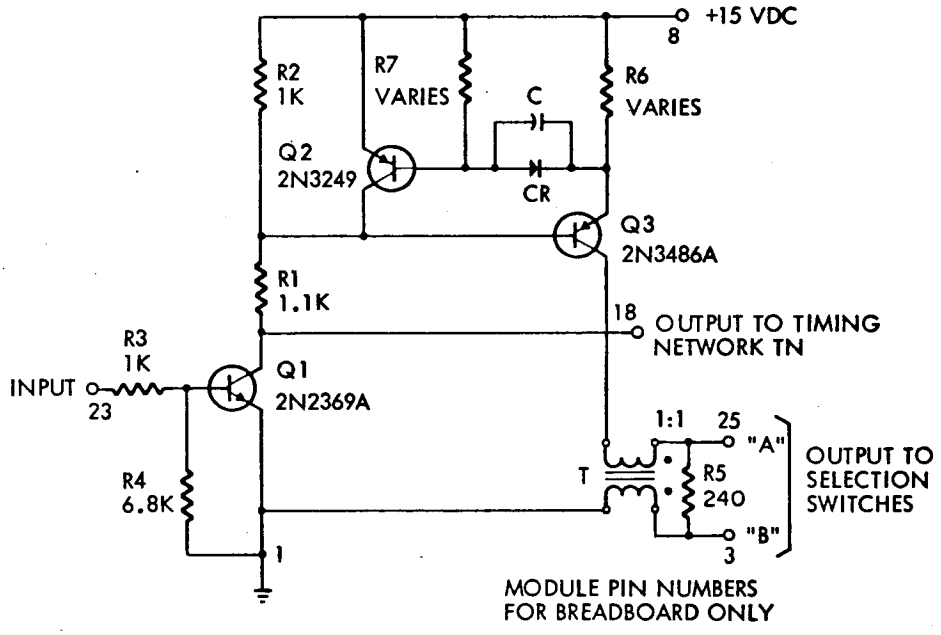


Figure 3.6-13. Word Pulse Generator Schematic

Design Details

A detailed analysis of this circuit has been performed to determine resistor values. A value of Re of approximately 6 ohms, and for Rb approximately 8000 ohms were found. The exact values must be selected according to the particular semiconductors used in each circuit.

Breadboard Module Evaluation

The current versus temperature slope was within 0.01 ma/°C of the ideal value for all combinations of worst case temperatures and voltages.

The actual current values were within 2 ma of the desired values at all combinations of worst case temperatures and voltages.

Current pulse rise time was 29 nsec minimum, 40 nsec maximum for all values of temperature and voltage.

Fall time of the current pulse was less than 60 nsec in all cases.

Pulse delay, as measured from the mid-point of the input voltage pulse to the mid-point of the output current pulse, was 40 nsec minimum, 50 nsec maximum for all values of temperature and voltage.

Parts Specification

Part	Breadboard	Prototype
R1, 1100 ohms	RC07GF112J	RC05GF112J
R2, 1000 ohms	RC07GF102J	RC05GF102J
R3, 1000 ohms	RC07GF102J	RC05GF102J
R4, 6800 ohms	RC07GF682J	RC05GF682J
R5, 2400 ohms	RC07GF242J	RC05GF242J
R_e, selected	RN60E	RN50E
R7, selected	RC07GF	RC05GF
Q1	2N2369A	2N2369A in TO-46 can
Q2	2N3249	2N3249 in TO-46 can
Q3	2N3486A	2N3486A
Diode	Fairchild FD6331	Microsemiconductor MC9853
Transformer	Technitrol	Pulse Engineering "Flat-Tran"

3.7 BIT COUNTER

The bit counter (figure 3.7-1) performs a number of functions for the memory system:

1. It remembers the particular bit within a word which is to be read or written at the time of the next clock pulse and increments automatically after that operation is complete. The counter may be reset to the Bit 1 position at any time by a Clear signal.

2. It provides the C selection switch function for the digit selection matrix. In the breadboard, 16 C leads (the prototype has 20) are switched by the bit counter to select a single C path for digit current (Write) or ON bias current (Read).

3. Five marker output pulses on selected bits are provided to external equipment which needs to monitor memory bit position. A marker output pulse is delivered shortly after the memory receives the clock pulse which causes it to Read or Write the particular bit so marked. The marker outputs are generated independent of word address.

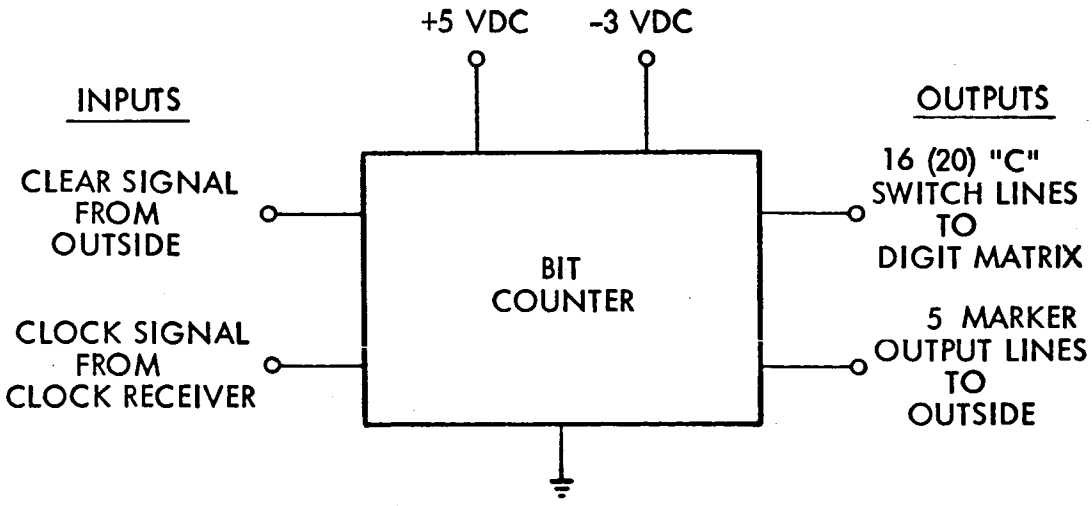


Figure 3.7-1. Bit Counter Elementary Diagram

Circuit Specifications

Conditions: The bit counter circuits function properly if the environments imposes conditions within the following limits:

Ambient temperature: -10°C to +85°C operating
-10°C to +139°C nonoperating
Power Supply Voltages: +4.5 to +5.5 volts DC
-2.7 to -3.3 volts DC
CLEAR signal passive level: -1.0 to +1.0 volts
active level: +2.0 to +6.0 volts
positive slope: no less than 5 mv per nanosecond over the range of uncertainty of +1.0 to +2.0 volts
duration: 1.2 microseconds minimum

Clock Signal trigger: To be recognized, the clock signal voltage must move negative by 4 volts or more at a rate of 20 to 400 millivolts per nanosecond.

Clock Signal non-trigger: In order to avoid counter advance, the clock signal must not move negative by more than 0.7 volt at a rate of more than 3 millivolts per nanosecond. Positive transitions will be ignored by the bit counter.

Input Signal Relationships: The leading edge of the Clear signal must not occur within the range of 1.2 microseconds before to 4.0 microseconds after a clock trigger (leading edge of clock signal). If the Clear signal is ON when the clock trigger occurs, it must go off no later than 1.2 microseconds after the clock trigger.

Repetition rate for clock triggers: 0 to 250 kHz.

Output load on Marker Outputs: Connecting circuits may take -10 to +10 ma from a marker output in the 1 state and may supply 0.1 to 10 ma to each marker output in the 0 state.

Output load on C switch leads: Connecting circuits may take 0 to 110 ma. from the selected C switch lead for the interval from 0.2 to 1.2 microseconds after the leading edge of a clock signal and 0 to 10 ma at other times. Connecting circuits may supply 0 to 50 microamperes to unselected switch leads.

Performance: The bit counter performs within limits specified below for all combinations of applied conditions within the limits specified above:

Positive Power Supply Loading: 0.9 ma during standby. During the MO output pulse (1.6 microseconds starting at a clock trigger) the circuit draws 17.5 ma to which must be added the currents equal to those supplied to the selected marker output and C switch lines. During the reset pulse (0.7 microsecond) which follows the MO pulse, the circuit draws 6.0 ma. During a reset pulse which follows the leading edge of a Clear signal, the circuit draws 8.4 ma; then 3.3 ma until the Clear signal falls back to its passive state. All values are nominal.

Negative Power Supply Loading: 0.4 ma during standby for each marker output line used. 1.0 ma total is added to this during the marker output pulse (1.6 microseconds) only.

Clear Signal Line Loading: No load for the "0" level. The bit counter circuits draw current from this line in the "1" state equal in milliamperes to the signal line voltage in volts minus 1.4 volts, ±20%.

Clock Signal line loading: Due to capacitive coupling, the clock signal line is loaded by this circuit only during transitions. When this signal falls at a rate of 100 mv per nanosecond, the bit counter will supply 4.7 ma (±20%) to the signal line; higher or lower fall rates result in a proportional change in current. Current drawn during positive transitions is variable, but does not exceed 0.8 ma for a 4-volt signal swing.

Marker Output Voltage: -0.1 to +0.5 volts for 0; +3.0 to +6.0 volts for 1.0

C Switch lead output voltage: On the selected lead, not less than 0.2 volt drop from positive power supply level at 100 ma output current; not more than 0.5 volt drop for any load current. Unselected leads are at 0 to +1.0 volts.

Marker Output Timing: A marker output pulse starts within 0 to 200 nanoseconds of the triggering edge of its clock pulse and has a duration of 1.2 to 2.0 microseconds. Rise and fall times are less than 300 nanoseconds.

Marker Output Selection: The five marker outputs may be connected to any desired subset of the 16 (20) bits in the counter. Only one marker output may be connected to any one bit.

C Switch Lead Timing: Only one of the 16 (20) leads is "selected" at any one time. The counter advances and the selection changes during the interval between 1.2 and 3.0 microseconds after the triggering edge of a clock pulse. The counter is reset and selection changes to Bit 1 lead during the interval 0 to 1.0 microseconds after the leading edge of a Clear signal. Except for these switching times, the C leads are stable during standby and between clocks.

Circuit Description

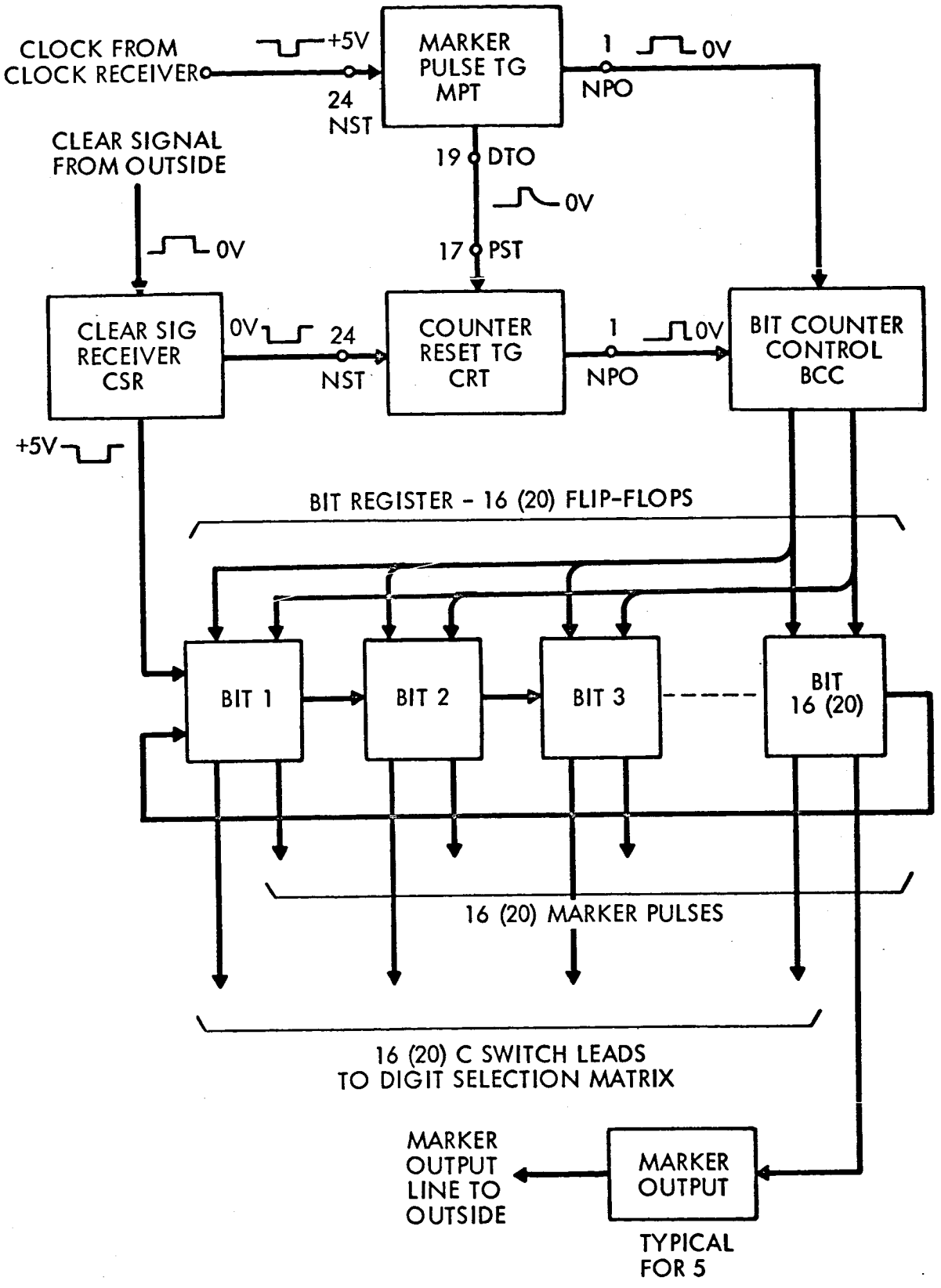
The bit counter is one of the few circuits in the memory which must draw power continuously between clocks and during standby. It must do this in order to remember which of 16 (20) bits is next up for action. If conventional symmetrical transistor flip flops were used, a minimum of four or five of them, all drawing power continuously, would be required. Instead, a complementary-transistor flip flop which uses power only in the 1 state has been designed for this application. By connecting 16 (20) of these flip flops as a ring counter (or shift register), bit position can be stored with only one flip flop ON and consuming power; standby power drain is minimized. The flip flop design also includes provision for driving the C switch leads to the digit selection matrix and for developing the bit marker output pulses required by equipment connecting to the memory.

The bit counter circuitry is shown in block diagram in figure 3.7-2; a timing diagram is shown in figure 3.7-3. The leading edge of the inverted clock pulse from the clock receiver triggers timing generator MPT, which generates a 1.6-microsecond marker timing pulse. During this interval, the normal output of MPT causes the bit counter control circuit BCC to increase C switch lead current-handling capability and to develop a 1.6 microsecond marker pulse, both at the previously-selected ON flip flop in the bit register. When MPT times out, it provides a trigger to the counter reset timing generator CRT which then starts a 0.7 microsecond reset pulse. The CRT normal output acts through bit counter control BCC to reset all bit register flip flops. At the same time, however, the trailing edge of the marker pulse at the previously-selected flip flop has started an RC-transient which tends to turn on the succeeding flip flop in the bit register. This transient outlasts the reset pulse from CRT and thus causes the succeeding flip flop to turn ON at the end of the reset pulse.

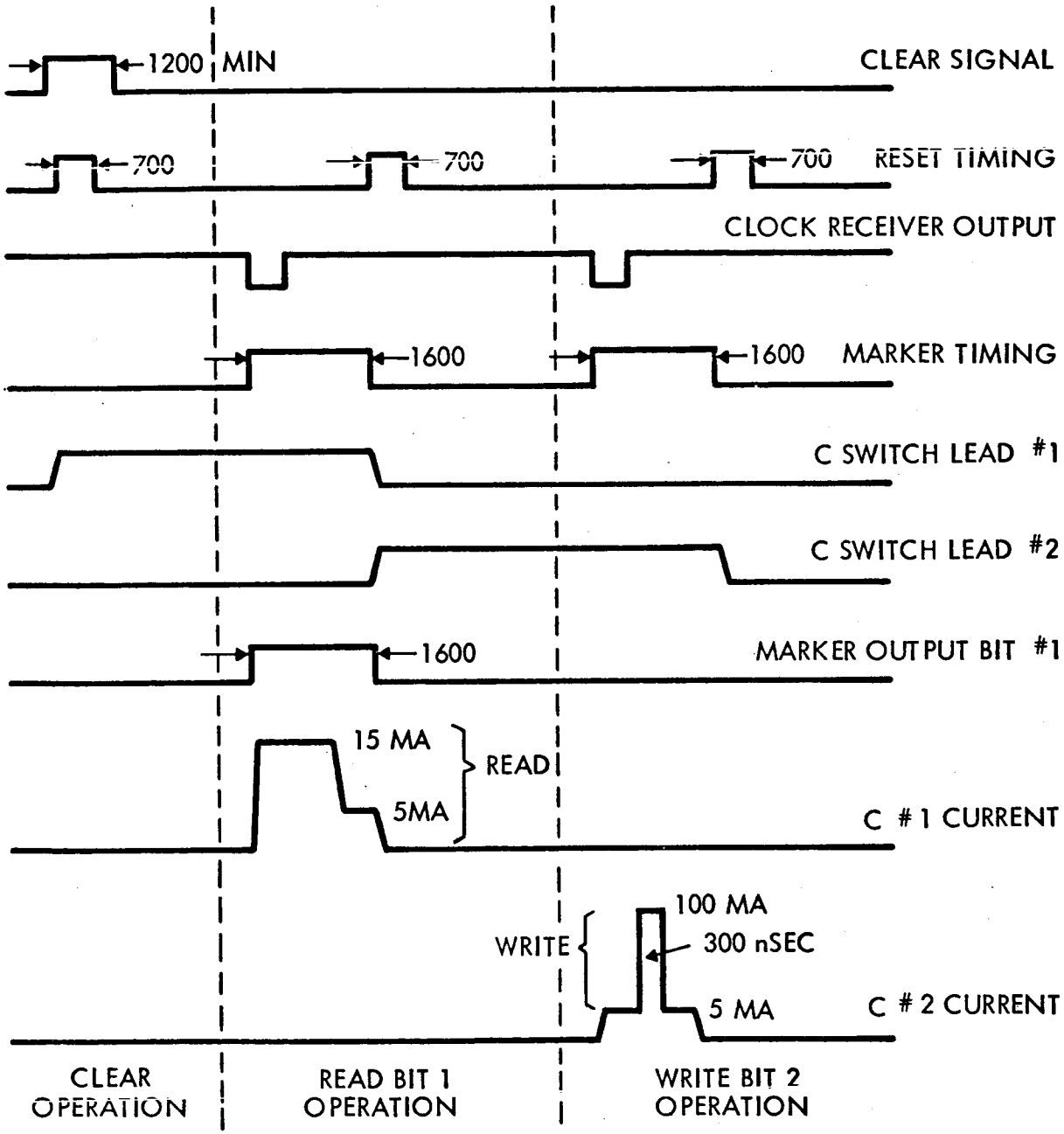
A standard DTL Clear signal from outside the memory is inverted by the Clear Signal Receiver CSR which triggers counter reset timing generator CRT and resets the bit register. CSR also supplies an ON signal to the bit 1 flip flop as long as the Clear signal remains high. It must do so until the 0.7-microsecond reset pulse is over to insure that Bit 1 turns on.

The marker pulses generated at the bit register flip flops do not have standard DTL-signal impedance characteristics. The five marker output stages may be connected as desired to the flip flops and they will then provide the proper output signal characteristics. In providing a low-impedance 0 level, the marker output circuits increase standby power dissipation of the memory by 1.0 mw for every one that is connected to a flip flop.

Timing generator circuits MPT and CRT are described in more detail in Section 3.8.1. In this application, these circuits are set for time delays of 1.6 and 0.7 microseconds, respectively. The bit register flip flop, bit counter control, clear signal receiver, and marker output circuits are described in Sections 3.7.1 through 3.7.4, which follow.



Figuer 3.7-2. Breadboard Bit Counter Block Diagram
(figures for prototype in parentheses)



NOTE: ALL PULSE WIDTHS IN NANOSECONDS

Figure 3.7-3. Bit Counter Timing Diagram

Packaging Notes

For the breadboard, two bit register flip flops and one marker output circuit are packaged in a single circuit module. For the prototype, it is expected that one bit register flip flop will be packaged with its associated portion of the digit selection matrix in a single module and that all five Marker Output circuits will be packaged together in a single module. The Clear Signal Receiver and the Bit Counter Control Circuit are packaged together in a single module for the breadboard; this will likely be done in the prototype also.

Breadboard Counter Evaluation

Temperature and voltage tests were conducted on an abbreviated (3 bit) bit counter. The circuits performed well at all combinations of temperature and voltage extremes.

Outlined below are some measurements of worst case variations in pertinent circuit parameters:

Bit Marker Output

Lowest "1" voltage output was +3.4V at T = -10°C, Vcc = +4.5V

Highest "0" output was in all cases less than 0.1V

Longest rise time: 30 nsec at Vcc = +4.5V, Vbb = -2.5V, T = -10°C

Longest fall time: 250 nsec at Vcc = +4.5V, Vbb = 2.5V, T = +85°C

Reset Pulse

Min reset pulse duration: 475 nanoseconds at +5.5V, +85°C

Max reset pulse duration: 2.5 microsec at +4.5V, -10°C

Max volatage change at "C" switch lead output due to digit current pulse of 130 ma = -0.4V, Vcc = +5.5V, T = -10°C

Propagation Delay

Max time as measured from fall of marker pulse to rise of stage being turned ON: 390 nanoseconds at Vcc = +4.5V, T = +85°C. 35 microamperes was injected into base circuit of shift transistors to simulate worst case leakage.

Bit Register Flip Flop characteristics measured at "C" switch lead output point:

Longest turn on time: 40 nsec at -10°C, +5.5V

Longest fall time: 450 nsec at +85°C, +5.5V

35 microamperes was injected into base circuit of shift transistors to simulate worst case leakage

3.7.1 Bit Register Flip Flop

The bit register remembers bit position within the 16-bit breadboard system word (20 for the prototype) between memory operations, provides the C switch lead drive for the digit selection matrix, develops bit marker pulses for external equipment, and advances under control of the Bit Counter Control circuit after each memory operation. The register is made from 16 (20) complementary-transistor flip flops (figure 3.7.4) in a ring counter (or end-around shift register) arrangement in which exactly one flip flop is always ON. The flip flop has been designed so that power dissipation is zero in the OFF state; the ON flip flop (and therefore the register) requires only 4.5 mw of standby power to remember bit position.

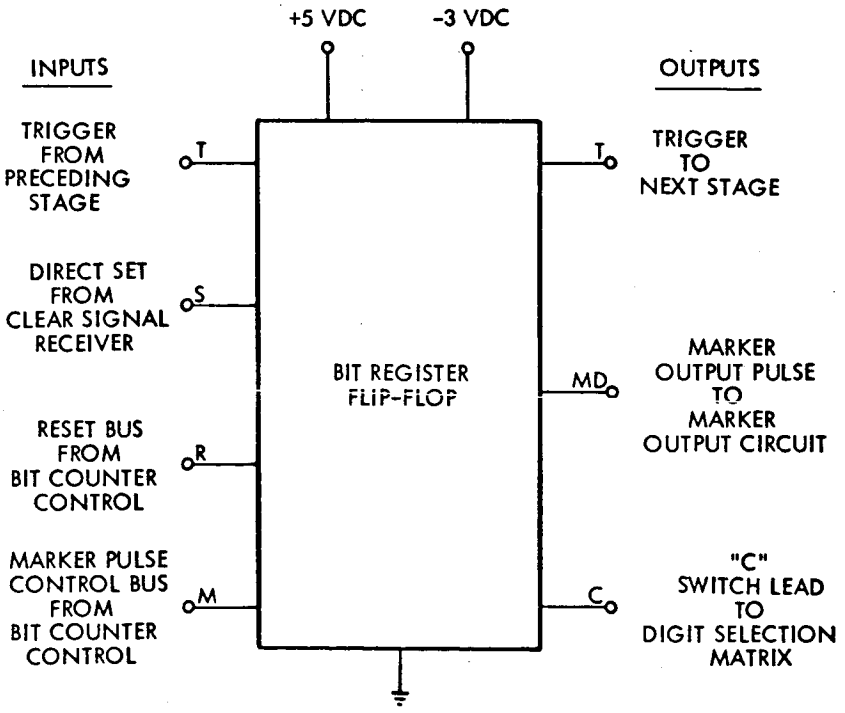


Figure 3.7-4. Bit Register Flip-Flop Elementary Diagram

The bit counter, which includes a number of control circuits as well as the bit register, is described in Section 3.7; the control circuits are described in Sections 3.7.2 through 3.7.4. The digit selection matrix is covered in Section 3.5.1.

Two bit register flip flops and one Marker Output circuit are packaged in a single module in the breadboard memory system; it is expected that a bit register flip flop with its associated section of the digit selection matrix will be packaged together in the prototype.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C
nonoperating: -10°C to 139°C
Power Supply Voltages: +4.5 to +5.5 volts DC
-2.7 to -3.3 volts DC
T or S Input current to trigger flip flop ON; 100 μa minimum from the circuit into the line for 30 nsec or more.
T or S Input current to NOT trigger: 20 μa maximum, same direction. No restriction for opposite direction.
T or S Input current to NOT reset: 100 μa maximum, from the line into the circuit.
R Input current to hold flip flop ON: 0.2 ma minimum, 20 ma maximum from the circuit into the line.
R Input current to provide full rated output capability: 3.0 ma minimum, 20 ma, maximum, same direction.
R Input voltage to hold flip flop OFF: 2.0 volts minimum, positive power supply voltage, maximum.
R Input voltage to reset flip flop: Positive power supply level minus 0.0 to 0.4 volts.
M Input current to produce marker pulse, flip flop ON: 0.8 to 2.5 ma from the circuit into the line. Rise time and fall time 0 to 100 nsec.
M Input voltage to NOT produce marker pulse, flip flop ON: Positive power supply level minus 0.0 to 0.5 volts.
M Input voltage to NOT produce marker pulse, flip flop OFF: 2.0 volts minimum, positive power supply level maximum.
T Output load: Capacitor, 120 to 180 pf. connected to positive power supply through two silicon back-to-back diodes.
MD Output load for "1": -0.2 to +10.0 ma from the circuit into the line
MD Output load for "0": -0.1 to -1.0 volts.
C Output load, flip flop ON, during marker pulse: 0 to 110 ma from the circuit into the line.

C Output load, all other times: -20 to +20 ma.
Duty Cycle: No restrictions.

Performance: This circuit performs within the limits specified below for all combinations of conditions within the limits specified above:

Positive power supply loading, standby, flip flop ON: 0.9 ma ±30%.
Positive power supply loading, during marker pulse, flip flop ON: 2 ma ± 30%plus the sum of currents flowing away from the circuit on all signal input and output leads.
Positive power supply loading, flip flop OFF: 20 ma, maximum.
Positive power supply loading, during reset pulse, flip flop being turned ON by T input: 0.9 ma ±30%.
Negative power supply loading, during standby: 0.33 ma ±30% if an MO circuit is connected to MD output; 0 ma if it is not.
Negative power supply loading, during marker pulse: 1.0 ma ±30%.
T Input voltage, during triggering: Drops at a rate of 5.0 to 9.0 mv per picocoulomb of charge withdrawn after an initial drop of 1.5 volts maximum from a voltage level held stable for at least 1.2 microsecond before triggering.
S Input voltage, flip flop ON: Positive power supply level minus 0.6 to 1.0 volts.
S Input voltage, flip flop OFF: Not less than positive power supply level minus 0.3 volt.
R Input voltage, flip flop ON: Positive power supply level minus 0.7 to 1.4 volts.
R Input current, during reset pulse: 10 microamperes maximum.
R Input current, flip flop OFF: 10 microamperes maximum.
M Input voltage, flip flop ON and during marker pulse: Positive power supply level minus 0.7 to 1.4 volts.
M Input current, all other times: 10 microamperes maximum from the line into the circuit.
T Ouput voltage, during marker pulse: Positive power supply level minus 0.9 to 1.5 volts.
T Output current: A minimum of 100 microamperes is pulled from the line by the circuit for at least one microsecond after the end of the marker pulse.
MD Output voltage for "1": +3.8 to +5.2 volts.
MD Output current for "0"" 200 to 500 microamperes from the line into the circuit.
C Output voltage, flip flop ON; Positive power supply level minus 0.0 to 0.5 volt.
C Output voltage, flip flop OFF: -0.3 to +0.3 volt.

Circuit Description

The bit register is formed by connecting a number of flip flops in a loop with the trigger output of each stage driving the trigger input of the next. Figure 3.7-5 shows a four-stage register.

The R input terminals of all flip flops are bussed and driven by a Bit Counter Control Circuit (Section 3.7.2); the M input terminals are connected in the same way. Only one flip flop in the register is ON at any one time; the position of the ON flip flop designates the bit count. The count is advanced by the Bit Counter Control circuit acting on the R and M busses. These busses also control the formation of the marker pulse and the enhancement of C-lead load handling capability, both at the ON flip flop only. The S input terminal is used to establish a known initial state of the bit register; it turns on a single stage while the R bus is pulsed to reset all other stages. See Section 3.7 for more details on timing and relationships between circuits in the complete bit counter.

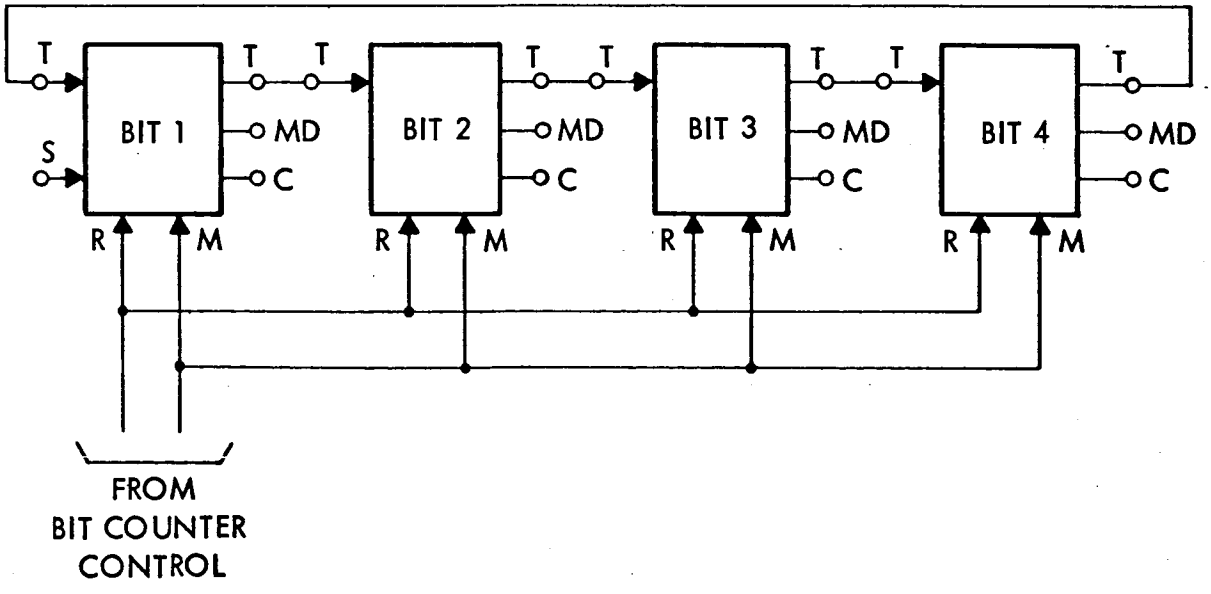


Figure 3.7-5. Four Stage Ring Counter

The flip flop consists of a complementary transistor flip flop, and an output buffer stage which develops the marker pulse and the propagation pulse which triggers the following stage of the bit register (see figure 3.7-6). The S, T, and R inputs all operate on the basic flip flop, which also provides the C switch lead output for the Digit Selection Matrix. The M control input operates on the buffer stage, which generates the other two outputs.

When the flip flop is off, all transistors are off (see the complete schematic, figure 3.7-7). The R bus is normally held at about +4 volts by the ON flip flop in the register, the M bus is normally held at +5 volts by the bit counter control circuit. No current flows on any input or output lead except possibly MD. If an MO circuit (Section 3.7.4) is connected to MD, it will hold the MD terminal at -0.5 volt and a small current will flow.

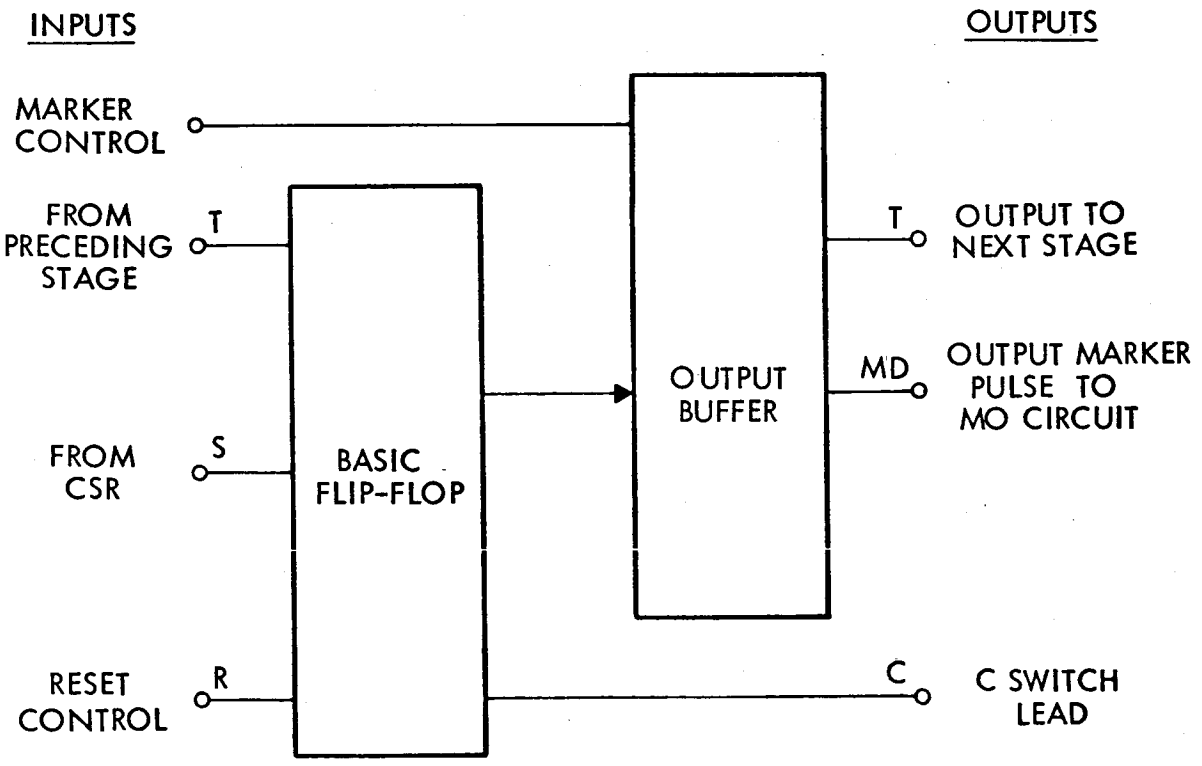
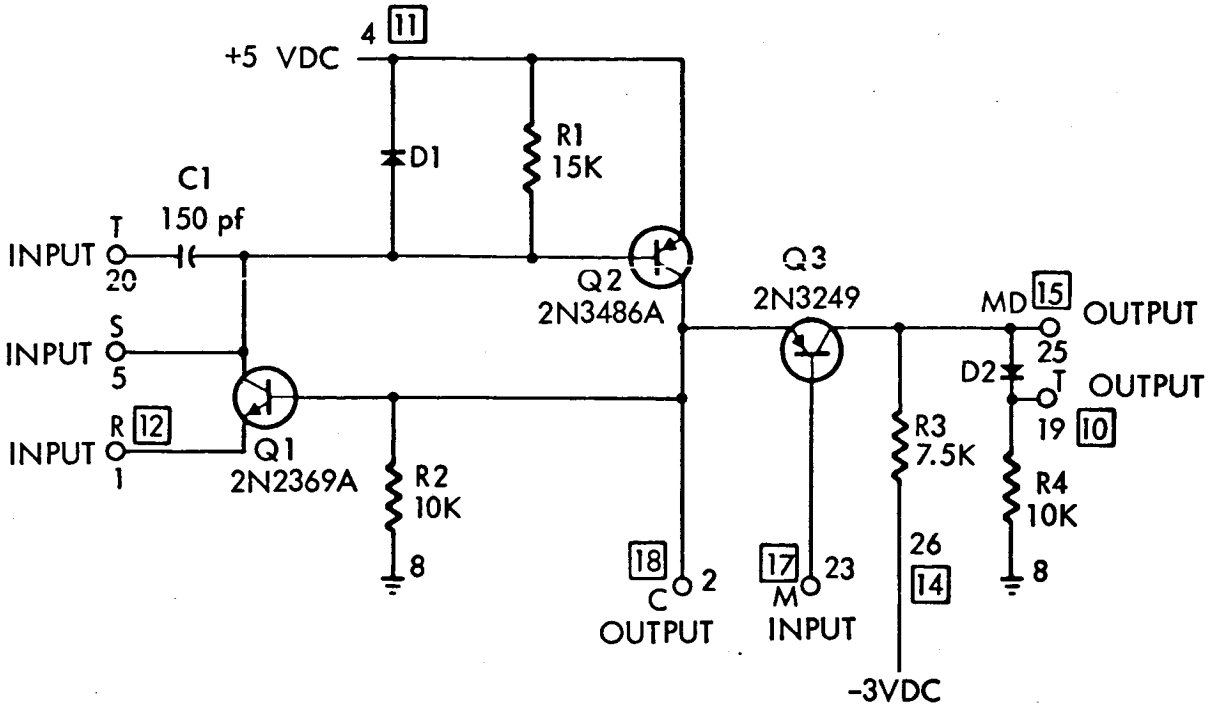


Figure 3.7-6. Bit Register Flip Flop Block Diagram



(PIN NUMBERS SHOWN FOR BREADBOARD)

☐ TERMINALS FOR SECOND FLIP-FLOP PACKAGED IN SAME MODULE

Figure 3.7-7. Bit Register Flip Flop Schematic

The flip flop is turned ON by pulling current from either the S or the T input terminal. This provides base current to Q2, which in turn tries to supply base current to Q1. The R control input is raised in voltage at this time by the bit counter control circuit to turn off the flip flop which was previously ON by back biasing all Q1 emitters in the bit register. When this reset pulse terminates, the current sink in the bit counter control circuit will pull current from Q1 which will then supply the Q2 base current after the input trigger current stops. The bit counter sinks a much larger current on the R lead during the marker pulse; this provides more base current to Q2 and permits it in turn to supply a 110 ma digit current pulse over the C lead.

The bit counter control also pulls current from the M terminal of an ON flip flop during a marker pulse. The M bus is clamped at +4 volts by the Q3 emitter diode in the ON flip flop, which prevents ON-biasing of Q3 transistors in the other OFF flip flops. When Q3 turns on, the MD terminal is pulled to +4 V to form the marker pulse for the marker output circuit. The T output terminal is pulled to about +3.5 volts in preparation for the trigger pulse to the following stage. This positive pulse does not affect the following stage; its input capacitor C1 quickly discharges through diode D1, with no effect on the flip flop. When the M bus again goes positive to terminate the marker pulse, Q3 turns off and R4 attempts to pull the T output back to ground level. Because of the reduced voltage on C1 in the following stage, that flip flop now gets a turn-on trigger while its input capacitor slowly builds back up to a normal voltage difference with current pulled by R4. The R4-C1 trigger transient must outlast the counter reset pulse placed on the R bus at this time by the bit counter control.

Design Details

Transistor Q2 has been allowed a cold old age beta of 40 for a Vce of 0.5 volts maximum at its maximum collector current of 120 ma. For standby, collector current is 0.5 ma and cold old age beta is 20 minimum. Transistor Q1 has a minimum cold old age beta of 20 during the marker pulse, 15 during standby. Transistor Q3 has a minimum cold old age beta of 30 for a Vce of 0.3 V maximum.

Parts Specifications

Part	Breadboard	Prototype
R1, 15,000 ohms	RC07GF153J	RC05GF153J
R2, 10,000 ohms	RC07GF103J	RC05GF103J
R3, 7,500 ohms	RC07GF752J	RC05GF752J
R4, 10,000 ohms	RC07GF103J	RC05GF103J
D1, D2	Fairchild FD6331	Microsemiconductor MC9853

Part	Breadboard	Prototype
Q1	2N2369A	2N2369A in TO-46 can
Q2	2N3249	2N3486A
Q3	2N3249	2N3249 in TO-46 can
C1, 150 pf	Sprague 5GA-T15	U.S. Capacitor C10A151K

3.7.2 Bit Counter Control Circuit (BCC)

The bit counter control (figure 3.7-8) circuit (BCC) drives two control lines which are common to all bit register flip flops. The M line controls the time-position of the edges of the bit marker pulse generated at the ON flip flop; the trailing edge of this pulse starts the transient which advances the count held in the register. The R line has two functions. It normally carries a small current which holds ON the flip flop marking present bit position. Current is increased in this line during the marker pulse interval (1.6 microseconds) in order to increase the current-handling capability of the selected C switch line to a level sufficient to carry digit write current (110 ma). Current is removed completely from

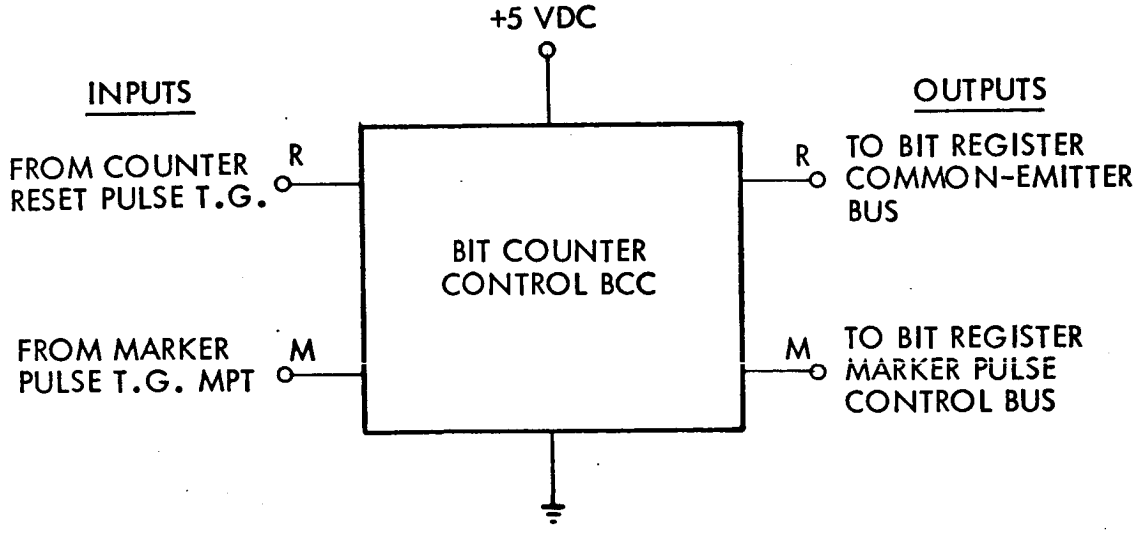


Figure 3.7-8. Bit Counter Control Elementary Diagram

the R line during the counter reset pulse (0.7 microseconds) which follows the bit marker pulse, to turn off the flip flop which was on and permit the advance of the bit count.

Inputs to the bit counter control circuit come directly from the NPO outputs of the marker pulse and counter reset pulse timing generators.

At the date of writing, the marker pulse control bus in the breadboard is split into two sections: Ma and Mb, each serving eight flip flops and driven from its own terminal in BCC. This split provides somewhat better control of leakage currents from the bit register, but its future is uncertain.

The bit counter control circuit and the Clear signal receiver (Section 3.7.3) are packaged in a single module in the breadboard and likely will be in the prototype also.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C.
nonoperating: -10°C to +139°C.

Power supply voltage: +4.5 to +5.5 volts DC.
Input signal voltage, inactive level: -0.5 to +0.3 volts.
Input signal voltage, active level: Positive power supply level minus 0.0 to 0.5 volts.
Input signal restriction: Only one input may be active at a time.
Output load, both outputs: Equivalent of a silicon diode with anode connected to a level of positive power supply voltage minus 0.0 to 0.5 volts.
Duty Cycle: No restrictions.

Performance: This circuit performs within limits specified below for all combinations of conditions within the limits specified above:

Power supply loading: Leakage currents only except during marker pulse when it is 2.0 ma ±20%.
R input signal loading: 1.0 to 1.8 ma from the line into the circuit while active, zero while inactive.
M input signal loading: 2.5 to 5.5 ma from the line into the circuit while active, zero while inactive.

R output current, circuit inactive: 0.27 to 0.54 ma from the line into the circuit.
R output current, during marker pulse: 3.2 to 10.5 ma from the line into the circuit.
R output voltage, during reset pulse: Positive power supply level minus 0.6 to 1.3 volts.
M output voltage, circuit inactive: Positive power supply level minus 0.0 to 0.5 volts.
M output current, dring marker pulse: 1.0 to 2.5 ma from the line into the circuit.
M output voltage, during reset pulse: Positive power supply level minus 0.0 to 0.5 volts.
Response delays: All turn-on delays 0 to 100 nsec. All turn-off delays 0 to 200 nsec.

Circuit Description

The marker pulse timing generator (MPT) drives a simple inverter stage in the bit counter control circuit (see figure 3.7-9) which in turn provides the current increments needed on the output lines during the marker pulse. Speed up capacitors are used across the resistors driving the marker control bus to help overcome output line capacitance and provide faster rise and fall times on the marker pulses.

A 10 K resistor R2 on the R output bus sets the standby current used to hold ON the flip flop in the bit register which is remembering bit position while the memory is inactive. During Reset, the counter reset timing (CRT) generator NPO output goes positive and supplies current to this resistor, which removes the holding current from the bit register and resets any ON flip flops. A diode prevents the bit counter control from turning on the counter reset timing generator when it is supposed to be OFF; a second diode prevents the off-biasing resistors on the marker control bus from supplying part or all of the flip flop holding current set by the 10 K resistor R2.

Design Details

Cold old age beta on the 2N2369A for a Vce of 0.35 volts is 16; circuit beta is actually much lower (about 4), primarily because the timing generator provides more precise timing if a fairly heavy current is drawn

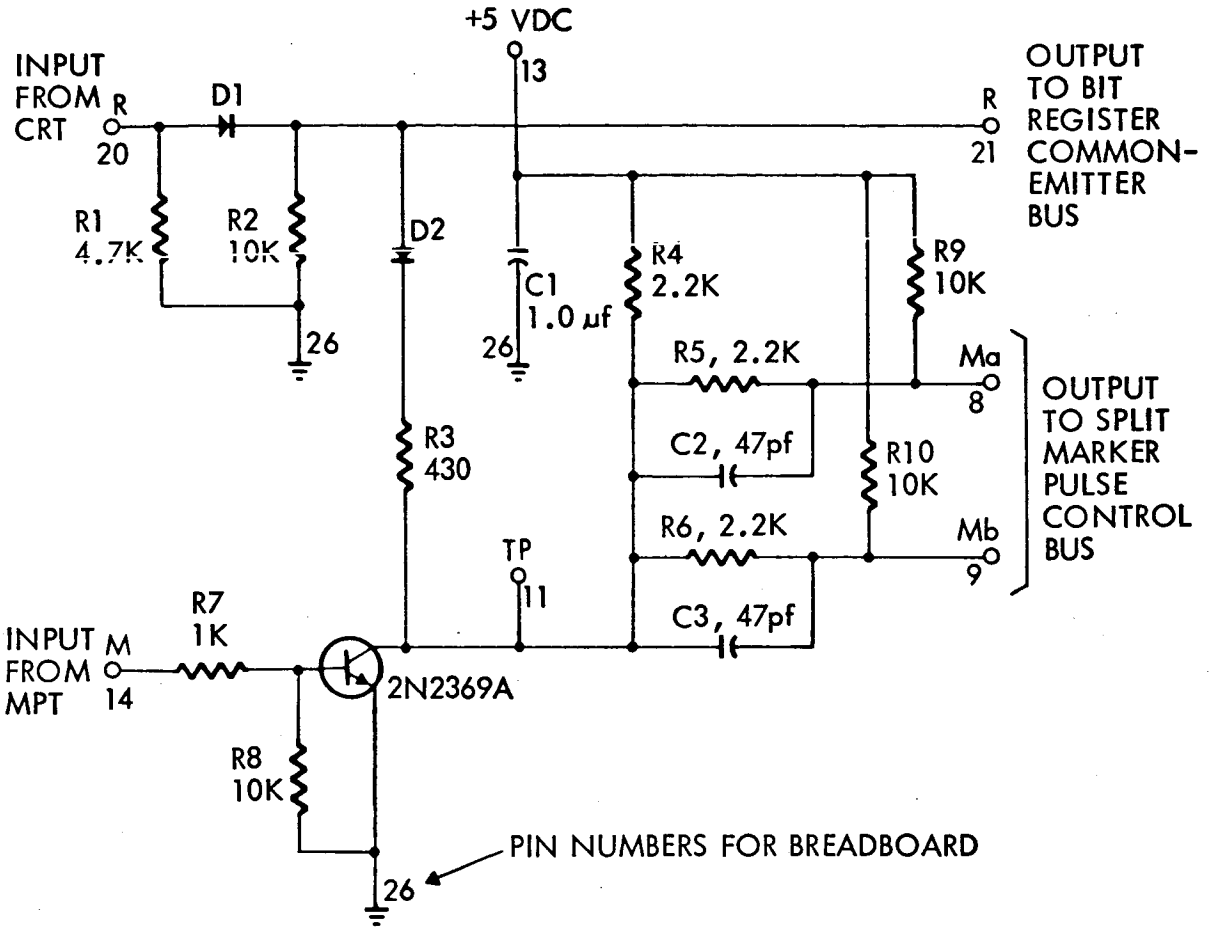


Figure 3.7-9. Bit Counter Control Circuit

from its output. The M input circuit has been designed to draw about 4 ma from the MPT timing generator.

Parts Specifications

Part	Breadboard	Prototype
R1, 4,700 ohms	RC07GF472J	RC05GF472J
R2, 10K ohms	RC07GF103J	RC05GF103J
R3, 430 ohms	RC07GF431J	RC05GF431J
R4, 2,200 ohms	RC07GF222J	RC05GF222J
R5, 2,200 ohms	RC07GF222J	RC05GF222J
R6, 2,200 ohms	RC07GF222J	RC05GF222J
R7, 1,000 ohms	RC07GF102J	RC05GF102J

Part	Breadboard	Prototype
R8, 10K ohms	RC07GF103J	RC05GF103J
R9, 10K ohms	RC07GF103J	RC05GF103J
R10, 10K ohms	RC07GF103J	RC05GF103J
D1, D2	Fairchild FD6331	Microsemiconductor MC9853
Transistor	2N2369A	2N2369A in TO-46 can
C1	CS13BF105K	CS13BF105K
C2, C3	Sprague 5GA-Q47	U.S. Capacitor C10A470K

3.7.3 CLEAR Signal Receiver (CSR)

The CLEAR Signal Receiver (CSR) (figure 3.7-10) connects to the CLEAR signal input line from external equipment and provides outputs to trigger the counter reset timing generator CRT and to turn on flip flop No. 1 in the Bit Register. In order to succeed in turning on Bit 1, the incoming CLEAR signal must be sustained until the CRT output pulse is complete which takes a nominal 0.7 microsecond. This has led to a minimum pulse width specification of 1.2 microseconds on the incoming CLEAR signal (see Section 3.7). The CLEAR signal receiver is packaged with the Bit Counter Control Circuit (Section 3.7.2) in the breadboard memory and probably in the prototype also.

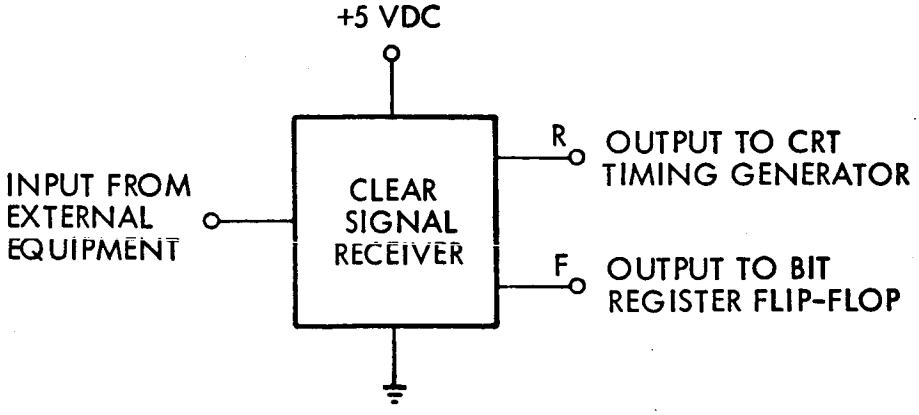


Figure 3-7.10. Clear Signal Receiver Elementary Diagram

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C.
nonoperating: -10°C to +130°C.
Power supply voltage: +4.5 to +5.5 volts DC.
CLEAR signal passive level: -1.0 to +1.0 volts.
active level: +2.0 to +6.0 volts.
positive slope: no less than 5 mv per nanosecond over the range of uncertainty of +1.0 to +2.0 volts.
R output load: Capacitance of 30 to 60 pf. Designed for Timing Generator NST input.
F output load voltage: +3.5 to +5.0 volts.
Duty Cycle: No restrictions.

Performance: This circuit performs within limits specified below for all combinations of conditions within the limits specified above:

Power supply loading: 1.2 ma ±30% while active. Leakage currents only otherwise.
CLEAR signal line loading: No load for passive level. The active level CLEAR signal is loaded by the equivalent of 1000 ohms returned to +1.4 volts with ±20% tolerance.
R Output current: The circuit will pull at least 1.0 ma from the R output line for at least 30 nanoseconds at turn-on.
F Output current: Circuit sinks 0.7 ma minimum from F output line while active, zero current while inactive.
Turn-on time: 100 nanoseconds maximum, measured from +1.4 volt level on input to current 50% point on F output.
Turn-off time: 300 nanoseconds maximum, same measuring points.

Circuit Description

This is a straightforward transistor inverter circuit, (figure 3.7-11). Diode D1 at the input is provided to improve the noise margin on the incoming CLEAR signal line in the "0" or passive state. Diode D2 prevents circuits connecting to the R output line from sinking current from circuits connecting to F output line. Resistor R1 discharges the input capacitor in the CRT timing generator after the Clear pulse. The circuit is designed and specified for a cold old age beta of 24 in the transistor.

Parts Specifications

Part	Breadboard	Prototype
R1, 3,300 ohms	RC07GF332J	RC05GF332J
R2, 1,000 ohms	RC07GF102J	RC05GF102J
R3, 10,000 ohms	RC07GF103J	RC05GF103J
R4, 3,300 ohms	RC07GF332J	RC05GF332J
D1, D2	Fairchild FD6331	Microsemiconductor MC9853
Transistor	2N2369A	2N2369A in TO-46 can

3.7.4 Marker Output Circuit (MO)

The marker output (figure 3.7-12) circuit (MO) buffers the marker pulse from a bit register flip flop without inversion and provides a signal with voltage and impedance characteristics suitable for driving any of the popular DTL and TTL integrated circuit logic elements in external equipment.

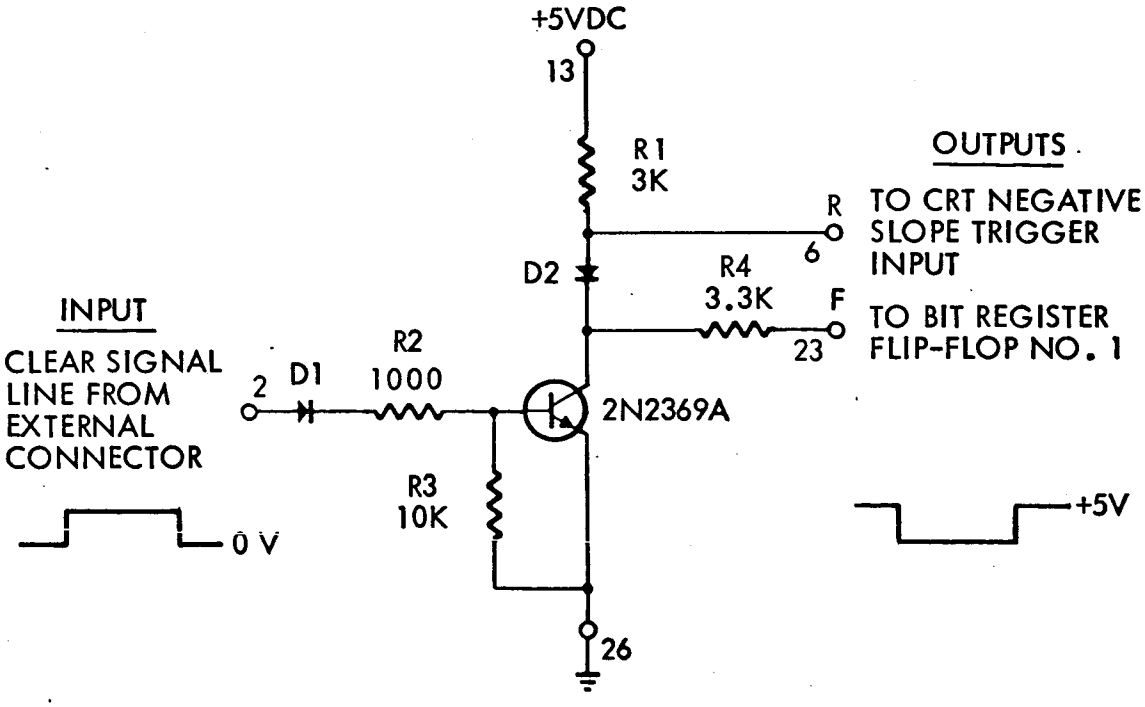


Figure 3.7-11. Clear Signal Receiver Circuit

120

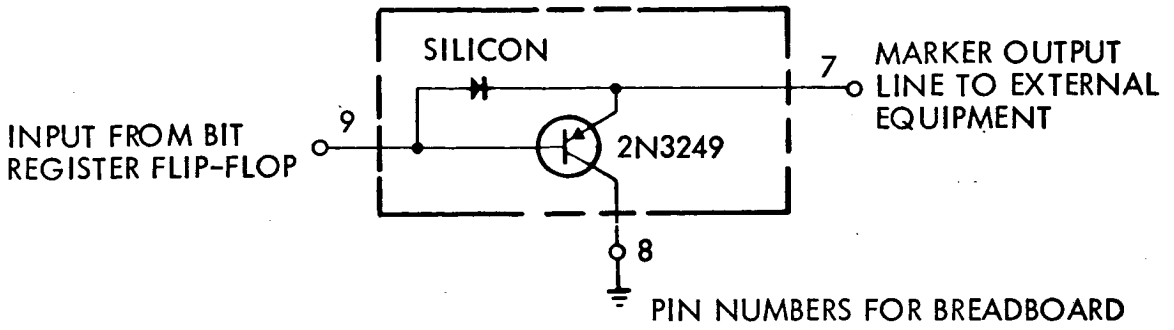


Figure 3.7-12. Marker Output Circuit

One marker output circuit is packaged with two bit register flip flops in the breadboard memory; five will be packaged together in a single module in the prototype. In both bases provision has been made for patching marker output circuits to any desired combination of bit register flip flops. Each marker output circuit which is connected increases standby power dissipation of the memory by 1.0 mw; this energy is needed to hold the marker output lines a a low impedance level in the passive or 0 state.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions with the following limits :

Ambient temperature, operating: -10°C to +85°C.
nonoperating: -10°C to +139°C.
Input signal current for "0": 200 to 500 microsamperes from the circuit into the line.
Input signal voltage for "1": +3.8 to +5.2 volts.
Input signal rise and fall times: 0 to 280 nanoseconds.
Output loading for "0": 0.1 to 10 ma from the line into the circuit.
Output loading for "1": 0 to 10 ma, either direction.
Duty Cycle: No restrictions.

Performance: This circuit performs within limits specified below for all combinations of applied conditions within the limits specified above:

Input signal voltage for "0": -0.1 to -1.0 volts.
Input signal current for "1": -0.2 to +10.0 ma from the input line into the circuit. Depends on output load.

Output signal voltage for "0": -0.1 to +0.5 volts.
Output signal voltage for "1": +3.0 to +6.0 volts.
Output signal voltage rise and fall times: 0 to 300 nanoseconds.
Output signal delay in relation to input signal: 0 to 10 nanoseconds, both edges.

Circuit Description

The circuit, as shown above, consists of a PNP emitter follower transistor which is permitted to saturate in the 0 state, and a discrete diode in parallel with, but poled opposite to, the base-emitter diode on the transistor. The discrete diode enables the bit register flip flop to drive marker output line capacitance during positive signal swings and eliminates the need for a pull up resistor on the output line, which, if used, would use power while the marker output line is in the normal "0" state. The collector diode of the transistor becomes forward-biased in the "0" state and prevents the input signal from pulling a lightly-loaded output line more negative than -0.1 volt. A minimum cold old age beta of 40 on the transistor has been calculated, and allowed for, in driving Vce down to 0.5 volt.

Parts Specifications

Part	Breadboard	Prototype
Diode	Fairchild FD6331	Microsemiconductor MC9853
Transistor	2N3249	2N3249 in TO-46 can

3.8 TIMING AND CONTROL CIRCUITS

A block diagram of the Timing and Control Circuitry is shown in figure 3.8-1.

3.8.1 Timing Generator (TG)

The Timing Generator Circuit (figure 3.8-2) is a pulse generator with versatile triggering inputs and several outputs. Six of these circuits are used in the breadboard system with output pulses varying in width from 270 to 1600 nanoseconds.

The normal pulse output is a positive 5-volt pulse, with the circuit capable of supplying appreciable current during the pulse. The inverted pulse output is normally at +5 volts; it sinks load current to ground level during the pulse. The delayed trigger output is quiescent until the trailing edge of the pulses generated on the other outputs; at that time it delivers a positive pulse which can be used to trigger other timing generators.

The NST and PST inputs are used to trigger the timing generator on falling and rising input voltage waveforms, respectively. The PTI input, when held at ground, prevents triggering of the circuit at the PST input.

This circuit uses no power when idle.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C.
nonoperating: -10°C to +139°C.
Power supply voltage: +4.5 to +5.5 volts DC.
NST input trigger: The inputs signal must move negative by 4 volts or more at a rate of 20 to 150 millivolts per nanosecond.
PST input trigger: The input signal must move positive by 4 volts or more at a rate of 20 to 150 millivolts per nanosecond.

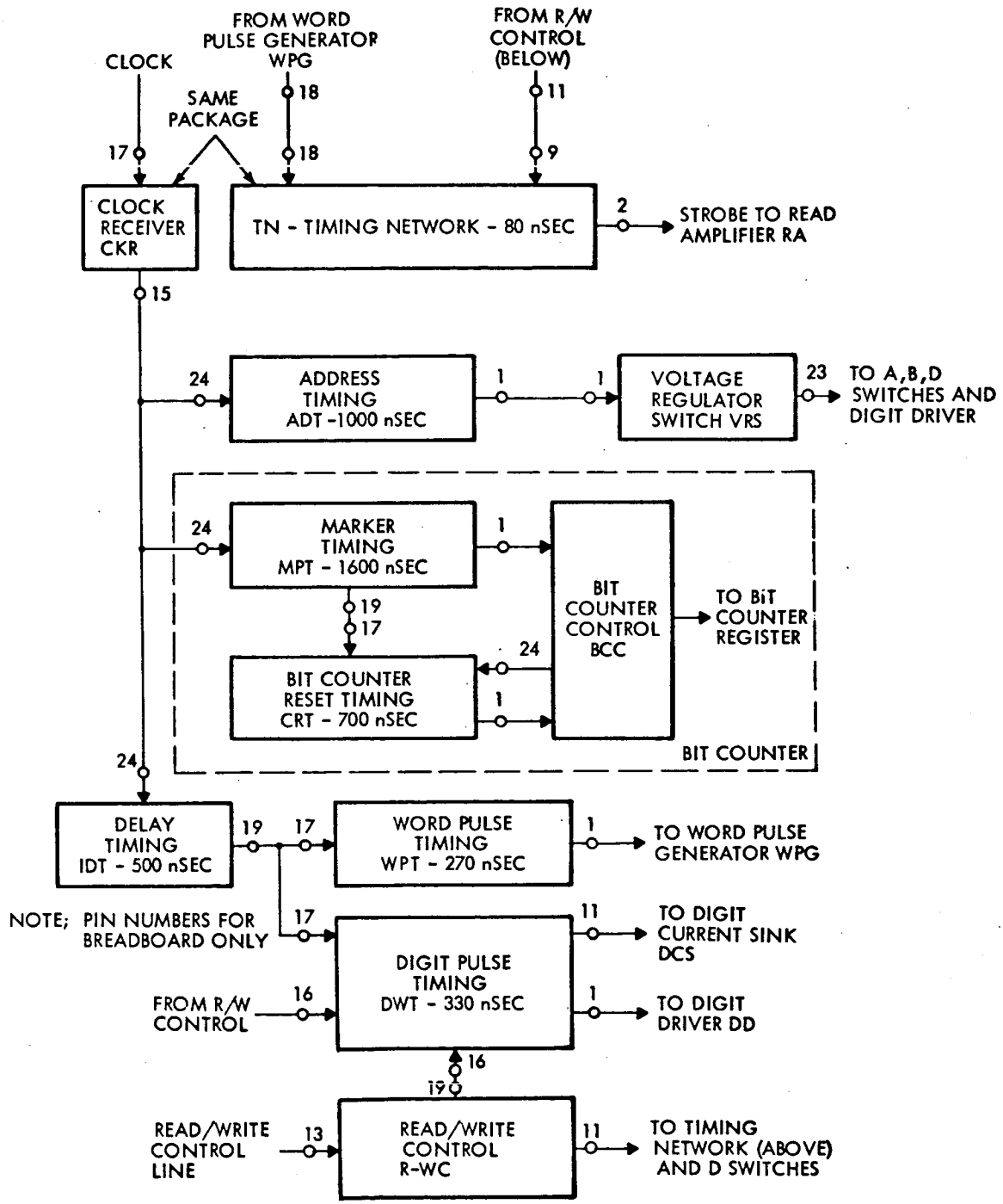


Figure 3.8-1. Timing and Control Circuit

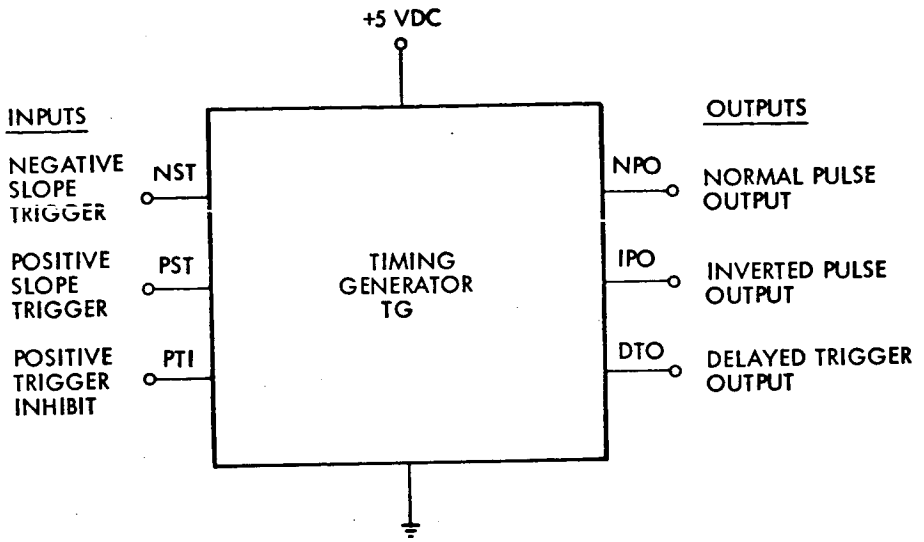


Figure 3.8-2. Timing Generator Elementary Diagram

NST input NOT trigger: Input line must not move negative by more than 0.7 volt at a rate greater than 3 millivolts per nanosecond.
PST input NOT trigger: Input line must not move positive by more than 1.5 volts at a rate greater than 3 millivolts per nanosecond.
PTI input to inhibit PST: -1.0 to +0.8 volts.
PTI input NOT to inhibit PST: +3.0 to +6.0 volts.
NPO output load, during the pulse: 0 to 10 ma from the circuit into the line.
NPO output load, standby: -30 to +30 microamperes.
IPO output load, during the pulse: 0 to 4 ma from the line into the circuit.
IPO output load, standby: -30 to +30 microamperes.
DTO output load, during trigger pulse: 0 to 20 ma from the circuit into the line.
DTO output voltage, other times: -0.5 to +0.5 volts.

Performance: This circuit performs within limits specified below for all combinations of conditions within the limits specified above:

Power supply loading, standby: Leakage currents only.
Power supply loading, during the pulse: 2.5 ma (±30%) plus NPO output load current.
Power supply loading, during delayed trigger pulse: 2.2 ma (±30%) plus DTO output load current.

NST and PST input loading: When the PST input rises (or the NST falls) at a rate of 100 mv per nanosecond, the circuit will draw from (supply to) the line 4.7 ma (±30%). Higher or lower rates result in proportional change in current.

PTI input load, while inhibiting PST input: 0 to 10 ma from the circuit into the line.

PTI input load, other times: Leakage currents only.

NPO output voltage, during the pulse: Positive power supply level minus 0.0 to 0.5 volt.

NPO output voltage, other times: -0.2 to +0.4 volt.

IPO output voltage, during the pulse: 0.0 to 0.5 volt..

IPO output voltage, other times: Positive power supply level plus +0.2 to -0.4 volt.

DTO output voltage, during trigger pulse: Positive power supply level minus 0.0 to 0.5 volt.

DTO output current, other times: -100 to +100 ma.

Main Pulse Duration:

Nominal Timing Capacitance C5	Duration
33*	200 to 270 nanoseconds
33	250 to 350 nanoseconds
68	480 to 620 nanoseconds
100	670 to 870 nanoseconds
120	800 to 1020 nanoseconds
220	1400 to 1800 nanoseconds

*with timing resistor R6 lowered from 10K to 7K.

Leading edge delay, main pulse: 0 to 30 nanoseconds.

Delayed trigger pulse width: 30 nanoseconds minimum.

Delay, main pulse trailing edge to trigger pulse leading edge: 0 to 10 nanoseconds.

Circuit Description

This circuit consists of a complementary transistor flip flop, an RC timing circuit, and a reset driver, shown in block diagram form in figure 3.8-3.

During standby the NPO output is at ground; the IPO output, and therefore the C5-R6 junction, are at the same level as the positive power supply. When the flip flop is triggered, NPO goes to +4.5 volts, and both sides of

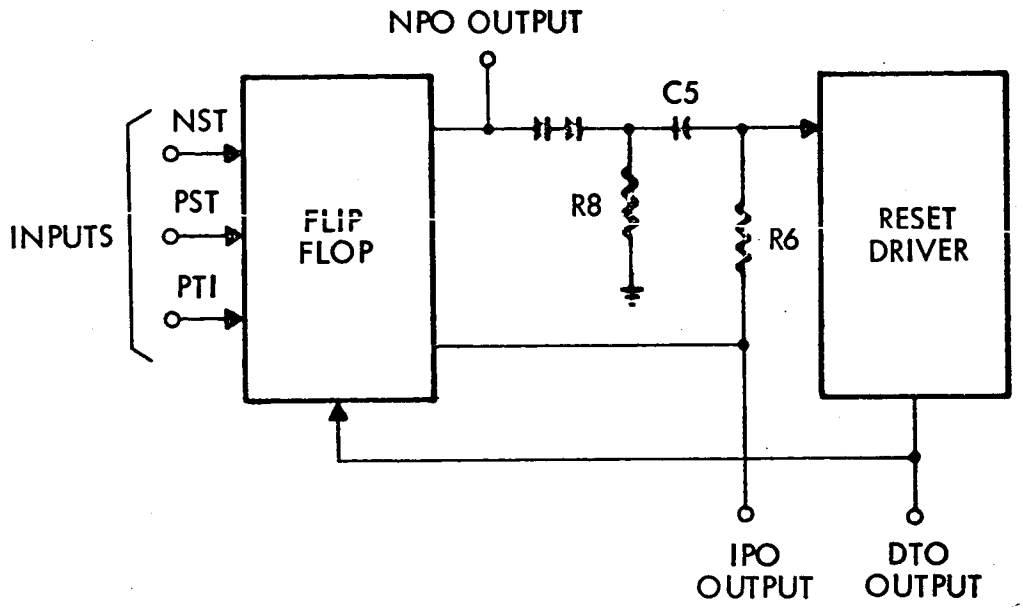


Figure 3.8-3. Timing Generator Block Diagram

capacitor C5 move positive by about 3 volts; the two diodes take up the difference of 1.5 volts. At the same time, the IPO output goes to ground level and R6-C5 start an exponential decay curve. The voltage at the R6-C5 junction at the leading edge of the pulse will be at 8 volts (assuming 5.0 volt power supply), and it follows a portion of an exponential curve which approaches 0.3 volt asymptotically. When this junction reaches 4.3 volts, however, the reset driver is activated and the pulse is terminated. The feedback loop which is activated when the reset driver starts to operate is regenerative: NPO and IPO start returning to normal levels and in so doing drive the reset driver ON hard. The leading edge of the DTO output pulse is consequently sharp and clean with risetime independent of the rate of decay on the C5-R6 junction voltage. The trailing edge of the output trigger pulse from DTO is determined by the C5-R8 time constant (the diodes are back biased) and, since no regeneration is provided, has a long fall time. Since C5 is adjusted for the desired desired main pulse length, the DTO output pulse length will vary also.

Stability of main pulse width is attained with this circuit by using a relatively short portion of the R-C exponential decay curve. The reset driver input threshold of 4.3 volts is attained while the current through R6-C5 is still greater than 50 percent of its initial value. Temperature and power supply voltage variation effects tend to cancel, causing relatively little variation on main pulse width. At high voltages and/or high temperatures, the initial voltage jump at C5 is greater, but the R6 current is greater too, so the C5-R6 junction voltage falls at a faster rate.

All transistors in this circuit are off when the circuit is inactive (see figure 3.8-4). The complementary flip flop Q1-Q3 may be triggered at either of two inputs; diodes D0 and D5-D6 prevent the inputs from resetting the flip flop. The positive trigger is inhibited if the PTI input is held near ground level; D7 drains away the trigger pulse coming in through C1 so that it does not get through D5-D6 to the basic flip flop.

The reset driver is a single PNP transistor. The reset pulse is coupled into the flip flop through diode D2, which normally isolates the two circuit sections. Speedup capacitor C2 insures a high gain regenerative feedback loop Q1-Q2 for the trailing edge of the main pulse. The flip flop Q1-Q3 provides positive feedback for the leading edge.

Three capacitors for C5 have been provided on the breadboard so that pulse width can be varied by changing connections at the module terminals. This will likely be done on the prototype also. Resistor R6 is shunted by 22K ohms for the shortest pulse width of 270 nsec.

Design Details

The equation for time delay is:

$$T = T_0 + (R6)(C5) \log_e \frac{\text{Initial R6 voltage}}{\text{Threshold R6 voltage}}$$

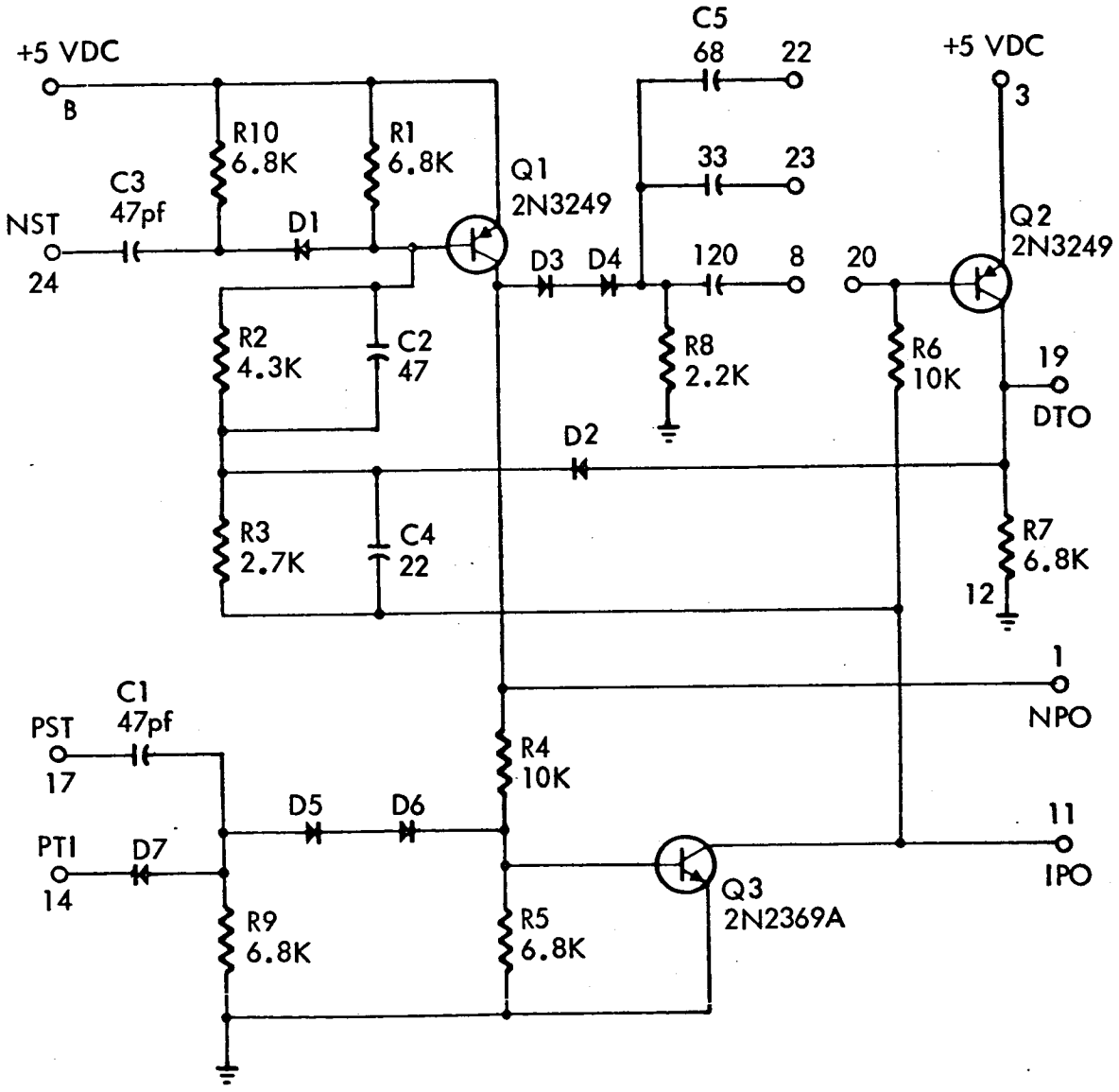


Figure 3.8-4. Timing Generator Schematic

The initial R6 voltage is the sum of the signal swigns on the NPO and IPO outputs minus the D3-D4 diode drops, and the threshold R6 voltage is the positive power supply level minus the base-emitter voltage on Q2 and minus the collector-emitter voltage on Q3. By substituting average values of all parameters including R6 = 10,000 and T_0 = 70 nsec, which is the result of transistor switching times and is empirically determined, a working equation is obtained:

$$T = 70 + 7\,(C5)$$ □□□□ (C5 in picofarads, T in nanoseconds)

In one application, R6 has been lowered to 7K to decrease the time delay below that obtained with the minimum C5 capacitor.

Minimum cold old age betas of 50 for Q1, Q2 and 24 for Q3 have been calculated and allowed for.

Breadboard Module Evaluation

Temperature and voltage tests were conducted on a timing circuit. The circuit performed well at all combinations of temperature and voltage extremes.

Outlined below are some measurements of worst case variations in pertinent parameters.

The circuit was loaded for these tests with:

A 430 ohm resistor to ground on the NPO output.
A 2000 ohm resistor to +5 volts on the IPO output.
C5 was 100 picofarads.

Time delay for a positive trigger ranged from 725 nanoseconds at +85°C, +5.5V to 765°nsec at -10°C, +4.5 volts.

Time delay for a negative trigger ranged from 750 nanoseconds at +85°C, +5.5V to 790 nanoseconds at =10°C, +4.5V.

Minimum positive trigger required: 2.4V step; risetime; 25 nsec, -10°C, +5.5V

Minimum negative trigger required: 2.9V step; risetime, 25 nsec, -10°C, +5.5V

Maximum delay from positive trigger to Q_1 ON: 13 nsec, -10°C, +4.5V

Maximum delay from negative trigger to Q_1 ON: 11 nsec, -10°C, +5.5V

Maximum delay from positive trigger to Q_3 ON: 8 nsec, -10°C

Maximum delay from negative trigger to Q_3 ON: 56 nsec, -10°C, +4.5V

Parts Specifications

Part	Breadboard	Prototype
R1, 6800 ohms	RC07GF682J	RC05GF682J
R2, 4300 ohms	RC07GF432J	RC05GF432J
R3, 2700 ohms	RC07GF272J	RC05GF272J
R4, 10K ohms	RC07GF103J	RC05GF103J
R5, 6800 ohms	RC07GF682J	RC05GF682J
R6, 10K ohms	RC07GF103J	RC05GF103J
R7, 6800 ohms	RC07GF682J	RC05GF682J
R8, 2200 ohms	RC07GF222J	RC05GF222J
R9, 6800 ohms	RC07GF682J	RC05GF682J
R10, 6800 ohms	RC07GF682J	RC05GF682J
Q1, Q2	2N3249	2N3249 in TO-46 can
Q3	2N2369A	2N2369A in TO-46 can
D1 - D7, inclusive	Fairchild FD6331	Microsemiconductor MC9853
C1, C2, C3, 47 pf	Sprague 5GA-Q47	U.S. Capacitor Corp. C10A470K
C4, 22 pf	Sprague 5GA-Q22	U.S. Capacitor Corp. C10A220K
C5a, 68 pf	Vitramon VK20CW680K	U.S. Capacitor Corp. C10A680G
C5b, 33 pf	Vitramon VK20CW330K	U.S. Capacitor Corp. C10A330G
C5c, 120 pf	Vitramon VK20CW121K	U.S. Capacitor Corp. C10A121G

3.8.2 Timing Network

The timing network (figure 3.8-5) is used to generate a narrow strobe pulse with a better and more reliable accuracy than that obtained with a Timing Generator circuit.

Referring now to the schematic, figure 3.8-6, the network consists of a bistable flip flop (Q2 and Q3) that is triggered ON to initiate and triggered OFF to terminate the strobe pulse. In the standby state Q1 and Q2 are off and use no power. The driver stage Q1 is gated to turn on only during a read operation.

The normal operation starts when Q1 is turned on. The voltage rise at the collector is differentiated through C1 and R8 to turn on Q2. As the collector voltage of Q2 drops it provides base drive to Q3. Q3 then turns on. This starts the strobe pulse, and supplies base current to Q2 through R14 to hold the flip flop ON.

The rising collector voltage of Q1 at turn-on is propagated through a delay line DL. Eighty nanoseconds later this voltage will appear at the terminating resistor R9 and couple through C4 to turn off Q3 and terminate the strobe pulse. With Q3 turned off, no sustaining base drive is available to Q2 and Q2 turns off. This completes the cycle.

The output pulse at the secondary winding of transformer T1 is 5 Volts at 12 ma for 80 nanoseconds. To support the voltage for 80 nanoseconds, the collector current driving the primary winding of T1 will be required to supply a transformer magnetization current in addition to the 12 ma output current. The transformer currents are shown in figure 3.8-7.

Magnetizing current is 6.6 ma for a worst case transformer inductance of 60 microhenries and collector current on Q3 is therefore about 20 ma. Cold old age beta on Q3 is figured at 40.

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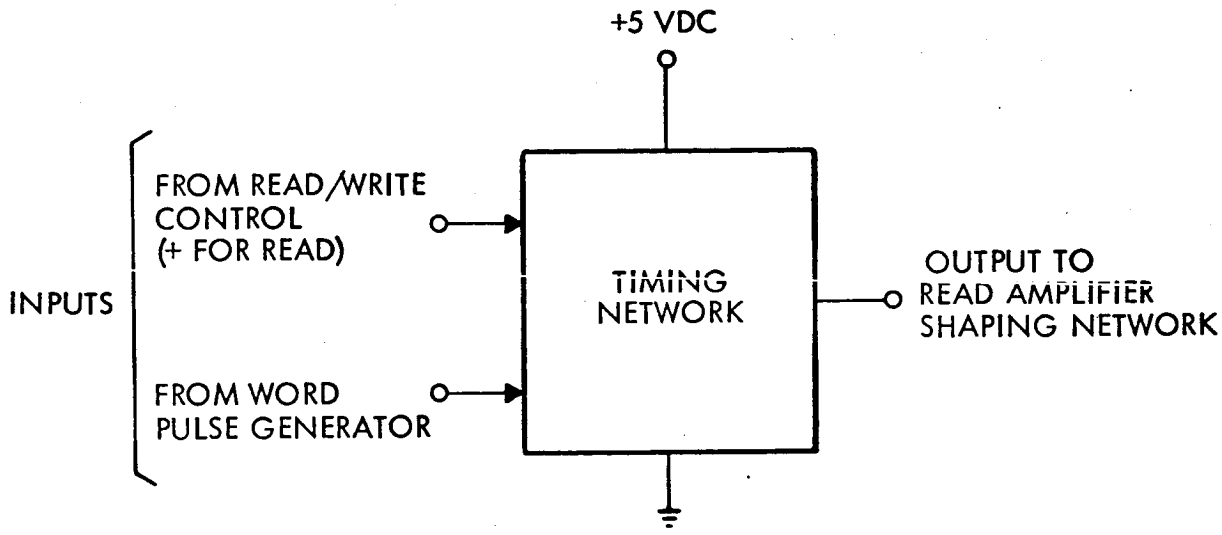

Figure 3.8-5 Timing Network Elementary Diagram

3.8.3 Voltage-Regulator Switch (VRS)

The voltage-regulator switch circuit (figure 3.8-8) provides an interruptable regulated power-supply voltage to the A and B word selection switches, Digit Driver, and D switches. Power is applied to these circuits within 100 nsec after a turn-on control signal is received from a timing circuit; turn-off response time is 200 nsec or less under most circumstances. The voltage-regulator switch circuit itself consumes no power when "OFF"; thus, the entire word selection system consumes zero power while the memory is in Standby. Even when the memory operates at its maximum rate of 100 kHz, power to the selection circuitry is applied through this circuit for only one microsecond in each 10-microsecond cycle, thus minimizing operating power drain.

The previously proposed design for this circuit included a special temperature-sensing element in order to achieve a constant regulated output voltage over the operating temperature range. This element, which is not readily available, has now been eliminated, and output voltage therefore changes with temperature. The variation takes place in a direction which partially compensates for temperature effects in the A

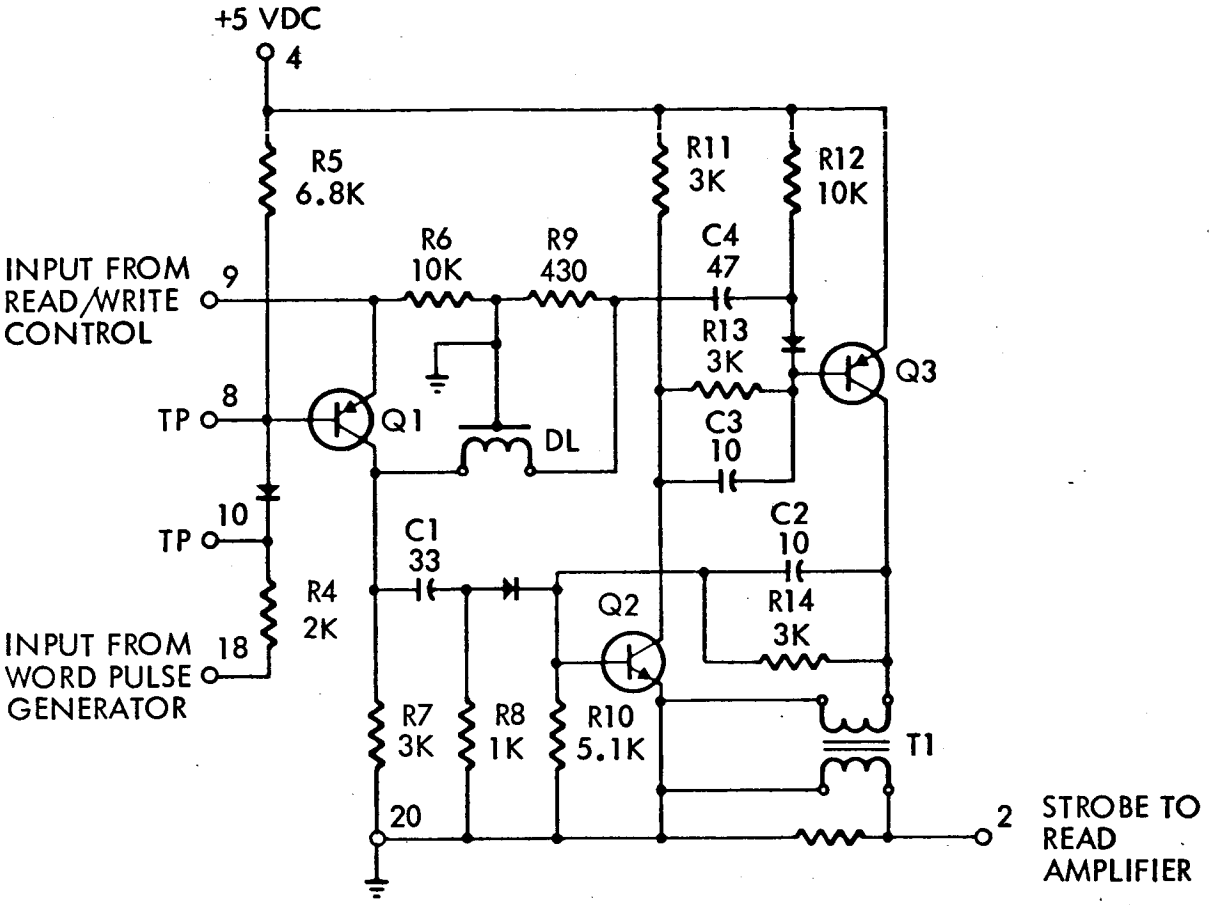

Figure 3.8.6. Timing Network Schematic

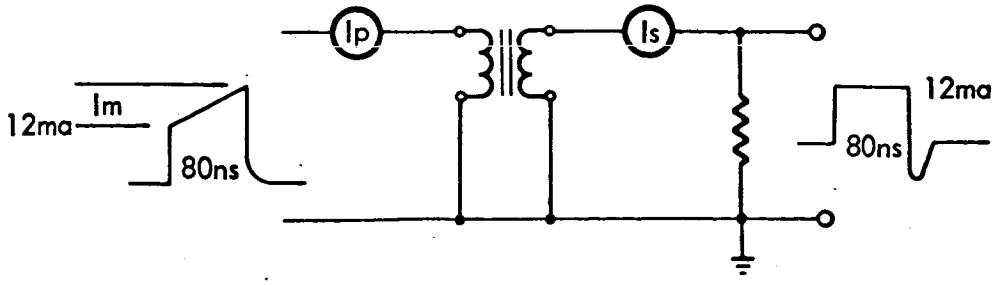

Figure 3.8-7. Timing Network Output Stage Waveshapes

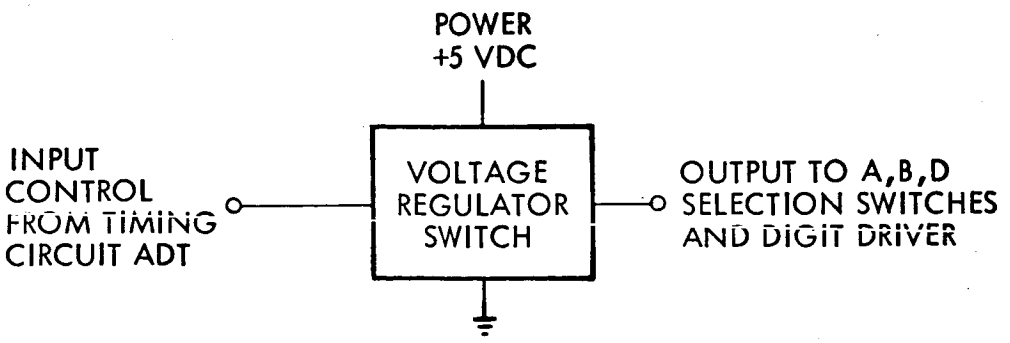

Figure 3.8-8 Voltage Regulator Switch Elementary Diagram

and B switches, and makes possible a more efficient switch design. Other changes in the circuit have eliminated the need for a -3 volt supply and have matched input signal requirements to the standard timing circuit outputs.

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature: -10°C to +85°C operating
-10°C to +139°C nonoperating
Power supply voltage: +4.5 to +5.5 volts DC
Input signal voltage, "ON" condition: +4.0 to +5.5 volts
Input signal voltage, "OFF" condition: 0.0 to +0.3 volts
Input signal voltage risetime: 0 to 100 nsec.
Output load (connected between output terminal and ground): 80 to 100 ma, measured at a load voltage of +4.0 volts.
Duty cycle: 0 to 100 percent.

Performance: This circuit performs within limits specified below for all combinations of applied conditions within the limits specified above:

Power supply loading, "ON" condition: 10.7 ma ±20 percent plus output load current.
Power supply loading "OFF" condition" Transistor leakage current only. Estimated at 1 ma at room temperature.

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Input signal load, steady-state "ON" condition: Circuit sinks 3.2 ma nominal, 5.0 ma maximum from the signal source.

Input signal load, "OFF" condition: Signal current is 0 ma when signal source is at 0.0 volts.

Output voltage, steady-state "ON" condition: Varies linearly with temperature. Guarantees are:
+3.9 ±0.1 volts at +25°C
+3.3 ±0.2 volts at +85°C
+4.3 ±0.2 volts at +10°C

Output current, "OFF" condition: Transistor leakage current only.

Turn-on time: Output voltage reaches 80 percent of steady-state amplitude in 100 nsec or less after the input pulse reaches 50 percent amplitude. Output voltage arrives and stays within steady-state specified tolerance limits within 200 nsec after input pulse reaches 50 percent amplitude.

Turn-off time: Output voltage falls below 50 percent point within one microsecond after input voltage falls below +0.3 volts. Under most conditions of temperature and power supply voltage this time is less than 200 nsec.

Circuit Description

The voltage-regulator switch circuit consists of a nonlinear bridge powered by the output voltage, a difference amplifier to detect bridge imbalance, and a series regulator controlled by the amplifier to drop the unregulated supply line voltage to the desired regulated level. The series regulator also switches the output off and on, as directed by the input signal acting through the amplifier. A simplified diagram is shown in figure 3.8-9.

Referring to the bridge circuit, the silicon diode forward voltage drop is nearly independent of current in the range of significant variation, but the voltage drops across the other three arms of the bridge are directly proportional to current. Consequently, the bridge is in balance for only one value of applied voltage. Any imbalance is detected and amplified by the difference amplifier and applied to the series regulator which immediately adjusts the output voltage in a direction which reduces the

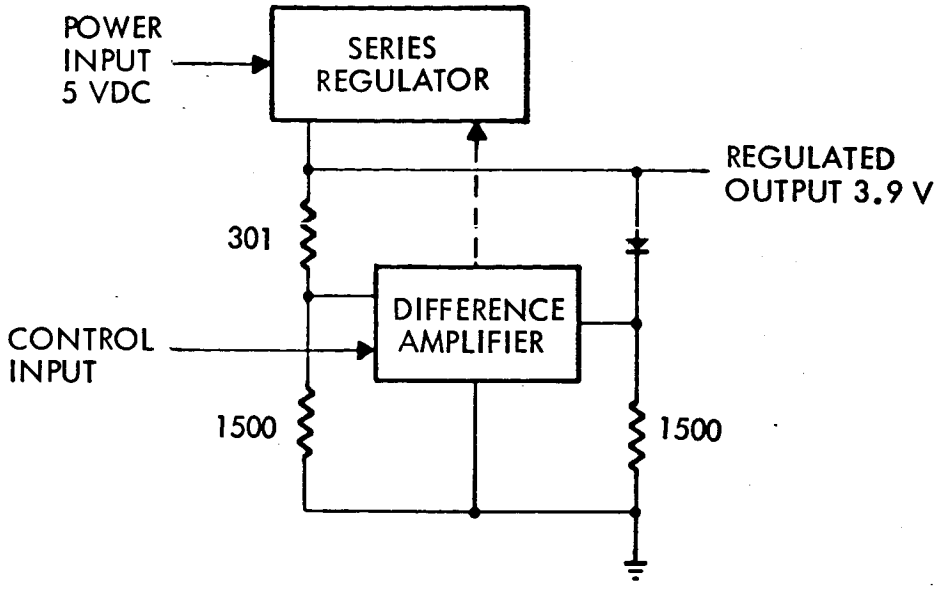


Figure 3.8-9 Voltage Regulator Switch Simplified Schematic

imbalance. With the resistor values shown, the output voltage will be six times the 0.65 volt forward drop of the silicon diode. Variations in diode forward characteristics may result in output voltage falling outside specifications when the circuit is initially assembled; it is brought within by shunting one of the bridge resistors on the left. Shunting the 301-ohm resistor with 8200 ohms raises the output voltage 0.1 volt; shunting the 1500 ohm resistor with 47,000 ohms lowers it 0.1 volt.

The forward drop of a silicon junction varies with temperature by about -2MV/°C, so that the 85°C drop is 120 MV less, and the -10°C drop is 70 MV more than that at room temperature. These changes are multiplied by the bridge ratio of six in computing output voltage change of the regulator circuit. Two second-order effects contribute to actual observed variations. The most important is a change in the way the difference amplifier loads the bridge.

Refering now to the complete schematic, figure 3.8-10, the series regulator transistor requires more base current at cold temperatures due to

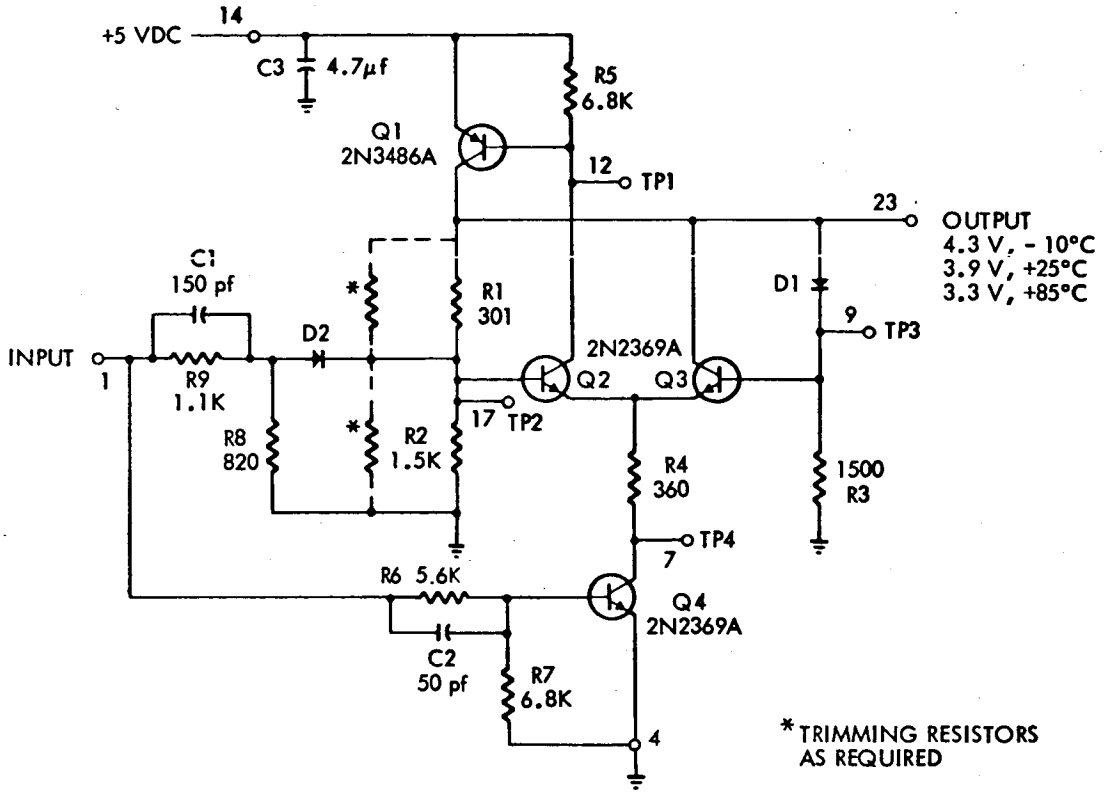


Figure 3.8-10 Voltage Regulator-Switch Schematic

reduction of beta and this, in turn, causes the difference amplifier to draw more base current from the left side of the bridge. This loading reduces the bridge ratio slightly, and thus the increase in output voltage at cold temperatures is less than expected. For the same reason, the decrease at high temperatures is also less. The other second-order effect comes from variations in diode current due to output voltage changes. This effect tends to increase output voltage changes as a function of temperature.

The regulator output voltage variation with temperature tends to compensate for loss of beta and increase in base-emitter voltages at cold temperatures in the A and B word selection switches. This has made possible a more efficient word switch design. To insure most efficient

use of available worst case voltage, the regulator circuit design permits the series regulator transistor to go into saturation at minimum voltage. A 0.2-volt saturation voltage allowance subtracted from the minimum power supply voltage of 4.5 volts thus defines the cold-temperature output voltage of 4.3 volts. A 0.2-volt tolerance on output voltage reflects the manufacturer's tolerance on saturation voltage of transistor Q1. At other voltages and temperatures Q1 is out of saturation; output voltage is independent of power supply voltage and falls linearly with increasing temperature.

The regulator circuit is turned off by transistor Q4 which opens the base current path for the series regulator transistor Q1. Transistor Q4 is biased on again when the input signal calls for power to be turned on, but this in itself does not force transistors Q1, Q2, and Q3 into conduction. A start up transient is also applied by the input signal to the base of Q2 to get the rest of the circuit active. A diode D2 prevents the start-up components from affecting the balance of the voltage sensing bridge.

Design Details

Transistor Q1 has a minimum cold old age beta of 54 for a Vce of 1.0 volt, but a circuit beta of 16 has been used so that it can be driven well into saturation under cold low-voltage conditions. A worst case initial Vce of 0.35 volts has been calculated when Q1 is receiving maximum available base current from the differential amplifier; the circuit specifications permit 0.4 volt maximum. The common emitter current of the differential amplifier is the maximum current available to the Q1 base; it is set at a cold nominal of 7 ma by 360 ohm resistor R4. Transistor Q4 is driven with a circuit beta of 14 to drive it down to a saturation voltage of 0.2 volt.

Metal-film resistors are specified in two places in the bridge to insure long-term output voltage stability. Speed-up capacitors are used in the input circuit to reduce turn-on and turn-off times. A filter capacitor on the input power lead reduces noise generation. Use of filter capacitors on the output lead cannot be permitted because of the need for rapid build-up of voltage on this bus for turn-on.

The peak worst case power dissipation of this entire circuit is about 100 mw. In its intended application, it will dissipate at this level for one microsecond and then be turned off for at least 9 microseconds. There is therefore no need to be concerned about power ratings on any of the components.

Breadboard Module Evaluation

The module assembled for the breadboard memory was tested at all combinations of temperature and voltage extremes. Correct operation was observed in all cases. Observed data:

Observed voltage, -10° C: 4.3V

Output voltage, +25° C: 3.9V

Output voltage, +85° C: 3.3V

Rise time 50 nsec, all cases

Fall time 170 nsec, all cases

Power consumption, 5V, 100 kHz, 25°C, 0.1 duty cycle:
6 mw excluding load and input signal power

Parts Specifications

Part	Breadboard	Prototype
R1, 301 ohms	RN60E3010F	RN50E3010F
R2, 1500 ohms	RN60E1501F	RN50E1501F
R3, 1500 ohms	RC07GF1525	RC05GF152J
R4, 360 ohms	RC07GF361J	RC05GF361J
R5, 6800 ohms	RC07GF682J	RC05GF682J
R6, 5600 ohms	RC07GF562J	RC05GF562J
R7, 6800 ohms	RC07GF682J	RC05GF682J
R8, 820 ohms	RC07GF821J	RC05GF821J
R9, 1100 ohms	RC07GF112J	RC05GF112J
C1, 150 pf	Sprague 5GA-T15	USCC C10A1510K
C2, 50 pf	Sprague 5GA-Q50	USCC C10A510K
C3, 4.7μf	CS13BC475K	CS13BC475K
D1, D2	Fairchild FD6331	Microsemiconductor MC9853
Q1	2N3486A	2N3486A
Q2, Q3, Q4	2N2369A	2N2369A in TO-46 can

3.8.4 Read/Write Control

The read/write control circuit (figure 3.8-11) receives the read/write control signal from external equipment. It develops outputs used to inhibit triggering of write timing generator DWT during a READ operation, to enable the D switch to supply ON bias current to the selected read amplifier input transformer primary for Read, and to inhibit generation of a strobe pulse in the timing network TN for Write.

This circuit is packaged with the Digit Driver in both breadboard and prototype memories. It uses one of four integrated circuit gates packaged in a single flat pack; the digit driver uses two others. Power to the integrated circuit is supplied by the voltage regulator switch only when the memory is active; standby power dissipation is zero.

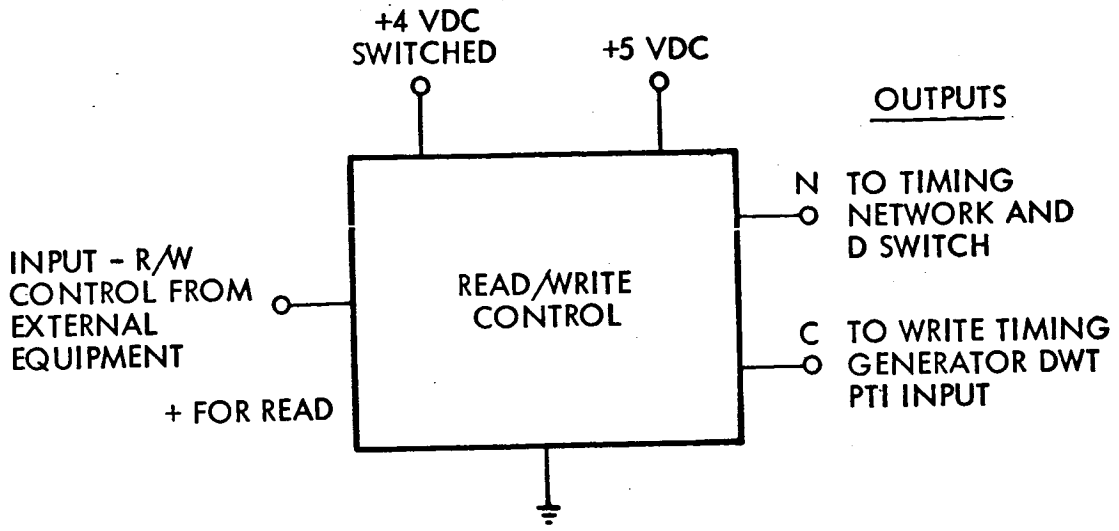


Figure 3.8-11 Read/Write Control Elementary Diagram

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C.
nonoperating: -10°C to +139°C.
Power supply voltages: +4.5 to +5.5 Volts DC
Switched power: +4.3 ±0.2 Volts DC at -10°C
+3.9 ±0.1 Volts DC at +25°C
+3.3 ±0.2 Volts DC at +85°C
Input voltage for READ: +2.2 to +8.0 Volts DC
Input voltage for WRITE: -0.5 to +0.9 Volts DC
N output load for READ: 0-15 ma from the circuit into the line
N output load for WRITE or for switched power OFF: -0.2 to +0.2 ma
C output load for READ: 0-8 ma from the line into the circuit
C output load for WRITE: or for switched power OFF: -0.1 to +0.1 ma
Duty Cycle: No restrictions.

Performance: This circuit performs within limits specified below for all combinations of applied conditions within the limits specified above:

+5VDC power supply loading for READ: 6.5 ma ±30% plus N output load current.

+5VDC power supply loading for WRITE or for switched power OFF: Leakage current only.
Switched power supply loading for READ: 4.7 ma ±30% (includes one unused gate in CS720J).
Switched power supply loading for WRITE: 3.1 ma ±30% (includes one unused gate in CS720J).
Input current for READ or for switched power OFF: less than 0.01 ma
Input current for WRITE and switched power ON: 1.5 ma ±50%, from the circuit into the line.
N output voltage for READ: Unswitched power supply level minus 0.0 to 0.5 volts.
N output voltage for WRITE or for switched power OFF: -0.3 to +0.3 volts.
C output voltage for READ: 0 to 0.5 volts.
C output voltage for WRITE or for switched power OFF: Within 0.5 volts of unswitched power supply level.
Response time: All outputs are within specification within 200 nanoseconds after switched power comes within specification turning ON.

Circuit Description

This circuit (figure 3.8-12) consists of an integrated circuit inverter which receives the input signal and drives the C output. The C output in turn drives a discrete PNP inverter stage which provides the N output.

The CS720J integrated circuit has a total of four gates (figure 3.8-13) two of which are used by the Digit Driver. The CS720J was selected because internal collector resistors are omitted on the outputs. This permits use of the unswitched positive power supply for the discrete PNP inverter and reduces the current load which would be placed on the voltage regulator switch if the entire circuit were connected to its output. No increase in power dissipation results because the PNP inverter can not draw current when power to the integrated circuit is switched OFF.

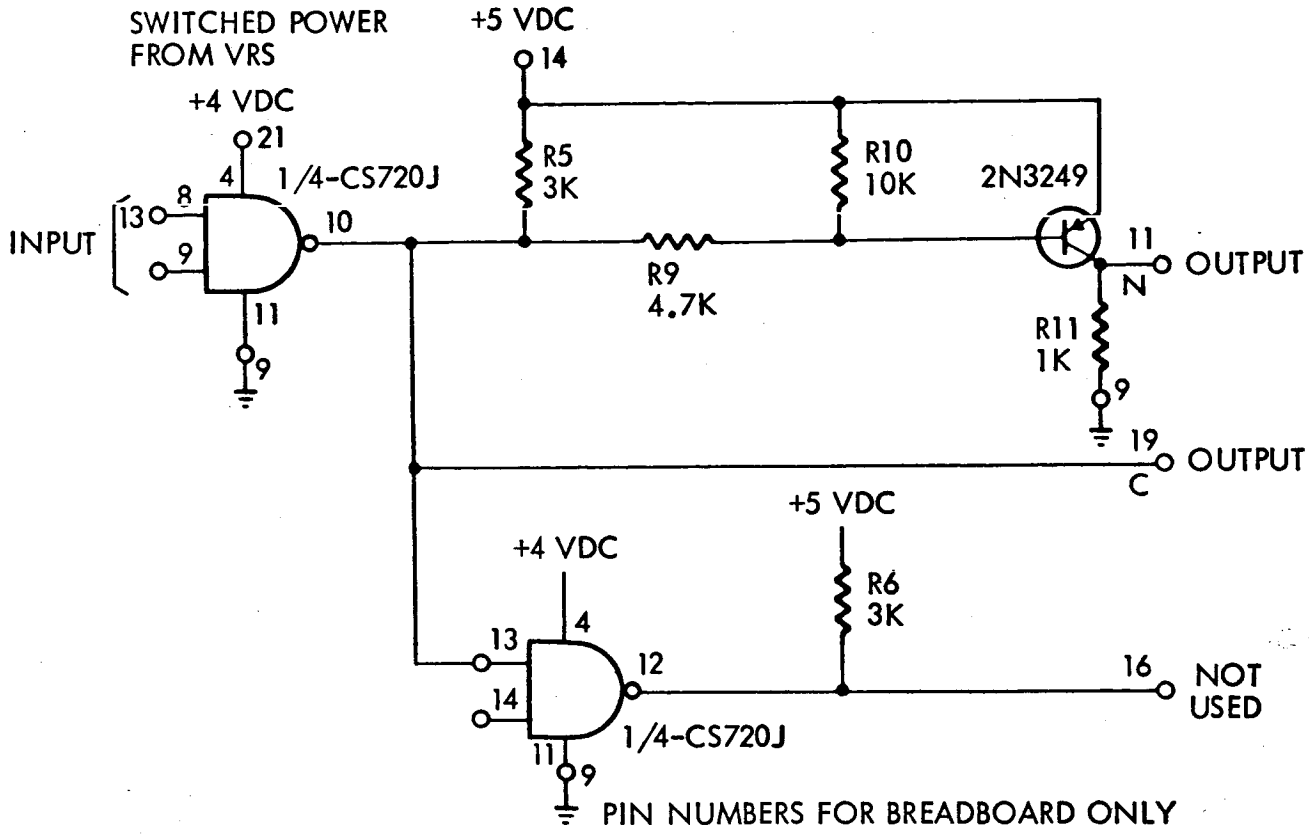


Figure 3.8-12 Read/Write Control Schematic

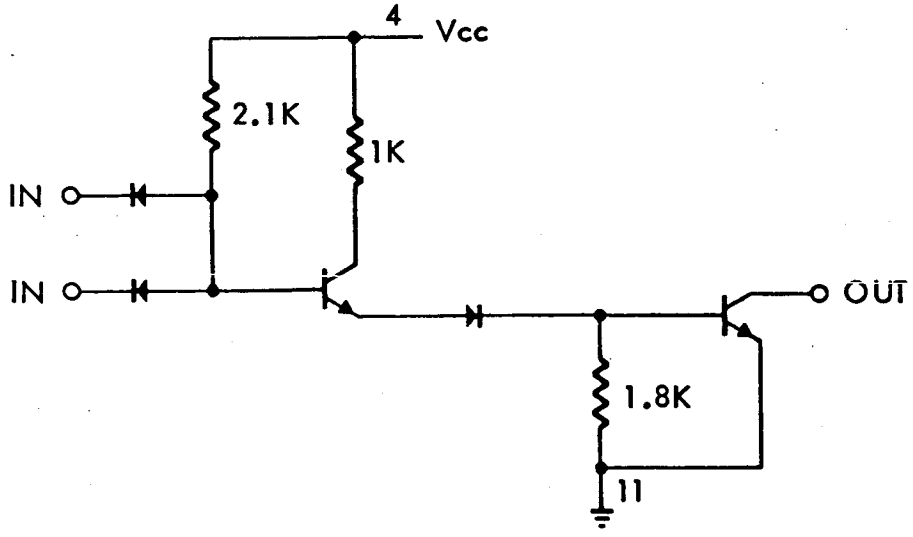


Figure 3.8-13 Typical C S 720 J Gate Schematic

Design Details

The discrete transistor has been allowed a cold old age beta of 40 at a Vce of 0.5 volt maximum. The manufacturer's data sheet indicates an initial room temperature upper limit on Vce of 0.27 volts under worst case circuit conditions.

Breadboard Module Evaluation

N output worst case delay from +4: 130 nanoseconds at -10°C, +4.5V
Worst case rise time: 100 nsec at -10°C, +4.5V.
Worst case fall time: 300 nsec at +85°C, +4.5V.

Parts Specifications

Part	Breadboard	Prototype
R5, 3,000 ohms	RC07GF302J	RC05GF302J
R6, 3,000 ohms	RC07GF302J	RC05GF302J
R9, 4,700 ohms	RC07GF472J	RC05GF472J
R10, 10K ohms	RC07GF103J	RC05GF103J
R11, 1,000 ohms	RC07GF102J	RC05GF102J
Transistor	2N3249	2N3249 in TO-46 can
Integrated Circuit	Signetics CS720J	Signetics CS720J

3.8.5 Clock Receiver Circuit (CKR)

The clock receiver (figure 3.8-14) is a simple inverter circuit which accepts the clock pulse from external equipment and provides, in turn, an inverted clock pulse to the bit counter marker pulse timing generator MPT, address timing generator ADT, and delay timing generator IDT.

As presently configured, the input to this circuit draws current from the input line in the 1 state. Although this represents a departure from the standard DTL-TTL interface, it has the significant advantage of permitting a design with zero power dissipation in the standby state.

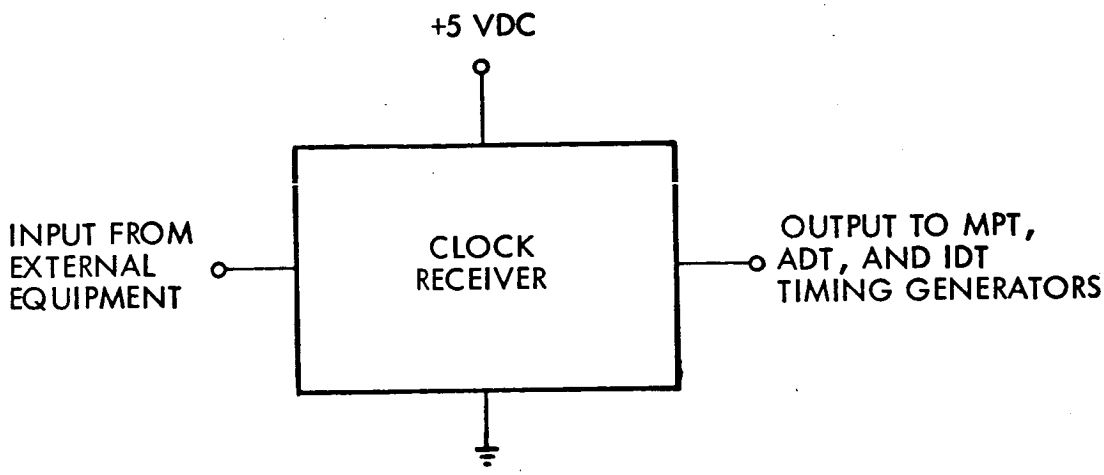


Figure 3.8-14 Clock Receiver Elementary Diagram

The clock receiver is packaged with the timing network in the breadboard memory. The complete schematic is shown in figure 3.8-15.

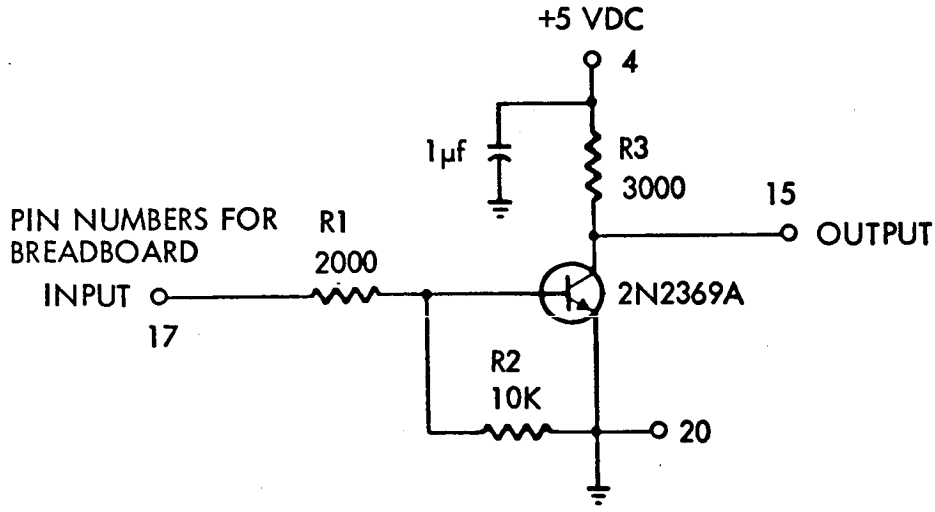


Figure 3.8-15 Clock Receiver Schematic

Circuit Specifications

Conditions: This circuit functions properly if its environment imposes conditions within the following limits:

Ambient temperature, operating: -10°C to +85°C
nonoperating: -10°C to +139°C
Power supply voltage: +4.5 to +5.5 volts DC
Input voltage for 0: -1.0 to +0.3 volts
Input voltage for 1: +1.7 to +6.0 volts
Input voltage risetime: Input voltage must cross the range of uncertainty of +0.3 to +1.7 volts at a minimum rate of 10 mv/nsec.
Output load: Capacitor of 100-200 pf.
Duty cycle: No restrictions; but input signal must remain in "0" state for at least 2 microseconds before transition to a "1" to permit capacitors in output load to stabilize.

Performance: This circuit performs within limits specified below for all combinations of applied conditions within the limits specified above.

Power supply loading, standby: Leakage currents only.
Power supply loading, input high: 1.5 ma ±30%.
Input line loading for "0": 0 ma at 0 V.
Input line loading for "1": Circuit pulls 0.5 ma at 1.7 V, 1.65 ma at +4 V, ±20%.
Output current: The peak current pulled from the line by the circuit is at least 4 ma during turn-on.

Design Details

Calculated minimum cold old age beta for the transistor is 24.

Parts Specifications

Part	Breadboard	Prototype
R1, 2,000 ohms	RC07GF202J	RC05GF202J
R2, 10K ohms	RC07GF103J	RC05GF103J
R3, 3,000 ohms	RC07GF302J	RC05GF302J
Transistor	2M2360A	2N2369A in TO-46 can
Capacitor	CS13BF105K	CS13BF105K

3.9 POWER CONSUMPTION

Power is specified with the nominal voltages of +15, +5, and -3 volt power supplies.

DEFINITION OF TERMS:

1. Standby power is defined as the power consumed during the absence of clock pulses with the system standing ready to receive them.
2. Operating power is the average power used when the system is operating at the maximum bit rate of 100,000 bits per second.
   a. Read Power: Average power as defined above, but in read mode only.
   b. Write Power: Average power as defined above, but in write mode only.

Table 3.9-1 is a summary of power used in each circuit with the total consumed power shown at the bottom. For comparison, table 3.9-1 also lists figures given in the original proposal.

The columns marked "calculated" are the powers consumed by the circuits based on the same rate of operation (100 KHz) that was used to calculate the power in the original proposal. This comparison shows that the calculated power is less than that proposed.

The discrepancy between the calculated and measured power, as given in the table, will now be explained.

Standby power: Calculated = 40 mw
Measured = 32 mw

The measured power is lower, due to lower than nominal dissipation in the Fairchild 702A integrated circuit in the Read Amplifier. The variation in power between units is large and a nominal total standby power of 30 to 40 mw may be expected.

Table 3.9-1. Power Summary

Circuit Name	Standby (mw)		Read (mw)		Write (mw)	
	Proposed	Calculated	Proposed	Calculated	Proposed	Calculated
Timing Circuits and Clock Receiver	7	0	18	27	18	20
Bit Counter	9	11	40	22	40	22
Digit Driver	0	0	0	2.3	5	6
"D" Switch & DCS	0	0	11	7	44	28
Digit Matrix	0	1.8	0	1.8	0	1.8
Read-Write Control	-	0	-	5	-	2.0
Read Amplifier	27	27	30	32	27	27
Word Pulse Generator	0	0	100	70	100	70
A & B Switches	0	0	26	38	26	38
Voltage Regulator Switch	0	0	5	16	5	16
Total Calculated	43	39.8	230	221.1	265	230
Actual Measured		32		240		270

Operating power:	Calculated, Read:	222 mw
	Measured, Read:	240 mw
	Calculated Write:	230 mw
	Measured Write:	270 mw

The measured operating power is higher than that calculated. This is because operating duty factors are higher than those used for calculations. The word read and digit write currents have a wider pulse width than intended. No attempt has been made to adjust pulse widths at this time. The prototype unit is expected to have pulses with the desired widths and this will result in lower measured power figures.

3.10 RELATIONSHIP OF BREADBOARD AND PROTOTYPE MODELS

The flight and prototype memory systems to be built under the present program will have 1024 "System" words of 20 bits each. External equipment will supply 10 bits of word address; the memory unit will remember bit address within the word and will operate on the bits in fixed serial progression. Because of considerations arising from the electrical characteristics of the woven plated wire memory element, the memory unit will be internally organized into 256 "memory" words, each 80 bits long. Eight of the externally supplied address bits select one of the 256 memory words; the remaining two address bits select one of the four "system" words in the 80-bit memory word.

The woven plated wire memory element provides the 256 x 80 matrix which allows access to the full memory capacity. The 256 words and 80 digits are arranged electronically in rectangular matrices. Notation and breakdown are shown by the following equations:

Memory capacity in bits = (A x B) x (C x D)
Prototype: 20, 480 = (16 x 16) x (20 x 4)
Breadboard: 4096 = (8 x 8) x (16 x 4)

For the prototype, selection of one of 16 A word switches and one of 16 B switches designates one of the 256 memory words; selection of one of 20 C switches (by the memory's bit counter) and one of 4 D switches

(by externally supplied address) designates one of the 80 bits in the designated memory word. For the breadboard, the numbers of A and B switches are each reduced by a factor of 2; the number of C switches is reduced from 20 to 16. The number of words is 64 instead of 256 and the number of bits per word is 64 instead of 80.

In brief, the breadboard memory has fewer A, B, and C switches and a smaller memory stack. In all other ways, the breadboard and prototype memories are electrically identical. Because of this close electrical similarity, the preceding descriptions of the memory system and circuits are equally valid for breadboard and prototype (flight) units. When the numbers of A, B, or C switches are cited for the breadboard, the numbers for the prototype are given in parenthesis.

No major electrical problems are forseen in building the full scale memory based on breadboard electrical design. Minor differences are as follows:

1. Each word in the prototype stack has 80 bits instead of 64; word inductance will be slightly higher, but this will probably be overcompensated for by the shorter wire lengths resulting from the much more compact prototype system packaging.

2. Each digit line in the prototype will have 256 words instead of 64, so digit line propagation delay will be about 12 nanoseconds instead of 3 nanoseconds. Both figures are negligibly small in relation to digit write pulse width of 300 nanoseconds and read strobe width of 80 nanoseconds.

3. Each B switch line will connect to 16 word lines in the stack instead of 8. This will double B line capacitance, and the increased word length will give another 25 percent increase. The B switch lines will, therefore, take longer to settle in voltage after switching. Because this is a very slow memory (by plated wire standards), a generous time has been allowed for B switch settling in the breadboard; it will probably be adequate for the prototype also.

4. Each A switch line will connect to 16 word diodes instead of 8 and capacitance will be increased by about 8 picofarads. This increase tends to slow the rise time of word pulse and thus reduce readback signal amplitude. However, 8 picofarads is a very small capacitance, and it is anticipated that total A line capacitance will be reduced by at least 8 picofarads because of the shorter lead lengths in the prototype.

5. The word pulse generator output busses will each connect to 16 A or B switches instead of 8. Additional capacitance due to the additional unselected switches will tend to slow word pulse risetime and slightly reduce the readback signal amplitude. Again, it is expected that this increase will be partially or fully compensated by shorter wire lengths in the prototype.

6. Each D bus pair in the digit selection matrix has 20 transformers instead of 16. This will result in slightly higher capacitances on the D busses; however, the effect will probably be cancelled by reduction of woring capacitance in the prototype package.

7. The common control lines to the bit register from the bit counter control circuit will connect to 20 flip flops instead of 16. Unselected stages contribute only capacitance, and the capacitance added by the additional stages in the bit register will be cancelled by reduction in wiring capacitance in the prototype.

8. Unselected A, B, C and D switches draw no power on standby, and standby power is unaffected; however, unselected A and B switches do draw power when the memory operates. At maximum speed (READ or WRITE), power dissipation will be about 6 milliwatts (or 3 percent) higher for the prototype.

Section 4

DESIGN AND FABRICATION OF THE BREADBOARD SYSTEM

4.1 PROGRAM GOALS FOR THE BREADBOARD MEMORY

The breadboard memory unit fabricated in Phase I of the present program is intended to demonstrate feasibility of a small, non-destructive readout, low-power, digital memory for space application based on woven plated-wire memory planes. More specifically, the phase I effort was addressed to the following:

1. Development of reliable memory circuits capable of operating over a temperature range of -10°C to +85°C.
2. Application of advanced electronic components, including integrated circuits, which appear to be likely candidates for qualification to flight hardware requirements.
3. Fabrication and successful operation from -10°C to +85°C of a breadboard memory unit using these circuits.
4. Demonstration of the low power consumption of a memory unit based on the previously proposed design approach.
5. Development of designs and fabrication techniques for packaging plated-wire memory planes for a space environment.
6. Demonstration of the adequacy of the memory plane packaging design by constructing a memory module to be operated as part of the breadboard system, but also to be tested separately in the vibration, shock, and decontamination environments likely to be encountered in space application.

In order to minimize costs in Phase I, the breadboard memory unit has only one-fifth the digital storage capacity of the flight hardware unit. Scaling down was done in a manner which would not eliminate any of the electrical problems which could be foreseen for the full-size unit. For a

more detailed comparison betweeen breadboard and prototype systems, see Section 3.10.

In Phase I no effort was made to package breadboard electronics modules in a form suitable for flight hardware.

4.2 PACKAGING CONFIGURATION

The breadboard package consists of an aluminum motherboard 12 inches by 15.25 inches into which plug the electronic circuits mounted in aluminum headers 1.56 inches by 1.09 inches, and the memory stack mounted on an aluminum header 5.00 inches by 6.75 inches. Individual insulated connector terminals press-fit into the headers and motherboard provide interconnection between header modules and motherboard. Interconnection between modules is by soldered wires on the back of the motherboard. The motherboard and the memory stack header were made by Elco-Pacific Corporation to Librascope drawings L300 003 659 and L540 001 915 respectively.

Figure 4.2-1 is a photograph of the completed breadboard assembly showing the motherboard, electronics modules, and memory module. The memory module (upper right hand corner) and the electronic modules are so arranged that digit/sense and word interconnections are short and orthogonal, resulting in minimum noise generation. Word select switches (WS) and the word pulse generator (WCD) are located in the nine modules at the bottom right in the photograph.

The three modules in the upper row to the left of the memory module are the read transformer RXF, read amplifier (RA), and the shaping network (SN), respectively. In the two columns below the read transformers and read amplifier are the 8 modules of the digit transformer matrix (DXF). In the two columns directly to the left of the transformer matrix modules are the 8 modules holding the 16 bit register flip flops (BC). Directly below the transformer matrix are the 4 "D" switch modules (DS). The two modules below the 2 "D" switches in the right hand column are the digit driver (DD) and the voltage regulator switch (VRS) respectively.

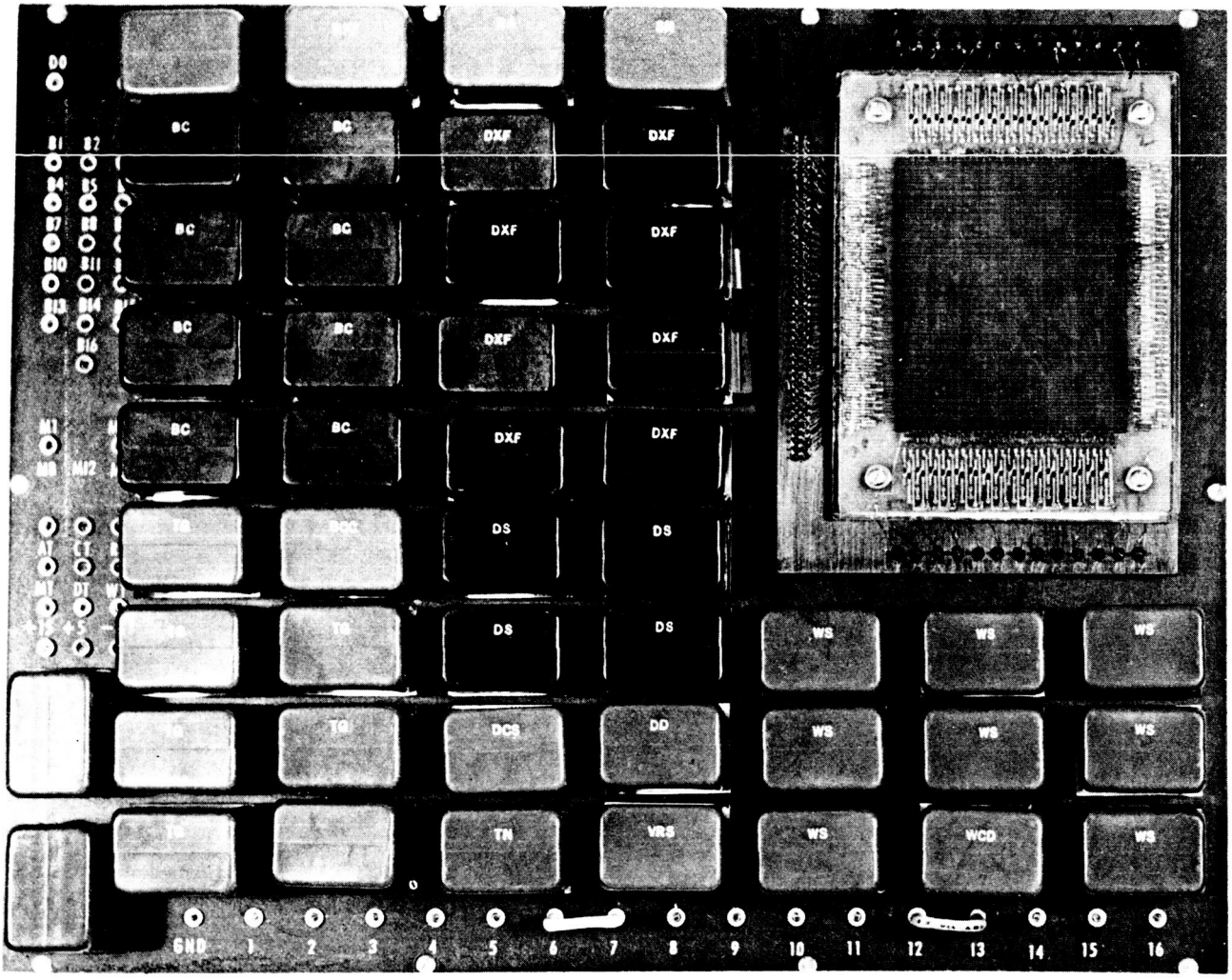


Figure 4.2-1 Breadboard Memory System

The two modules along the left edge are modified for use as cable connectors for interconnection with the memory exerciser. The rest of the modules (lower left) are the timing generators and timing network. Test points, connected to selected timing and signal waveforms, are provided along the bottom and left hand edges.

4.3 MEMORY STACK PACKAGING

4.3.1 Goal

The memory stack package has been recognized from the beginning by both Librascope and JPL to represent the most critical packaging design problem in the Low-Power Space Memory System. For this reason the breadboard stack design has been aimed at meeting the specifications for flight hardware set down by JPL. Librascope conducted an exploratory temperature-vibration test in early 1965* to get a feel for the nature of environmental protection that is required for the memory mats. The resules of that test were very useful in all phases of the JPL contract. It was found that the only real environmental problem was the supporting of small wires, particularly spring loops, so they do not have the opportunity to resonate.

A potting study was performed to determine what effects various types of embedment material have on the electrical characteristics of the mat. This test showed the embedment material should have the following characteristics:

1. The material should not transmit thermal strain to the plated wire.
2. The material should be resilient so that it is a source of vibration damping.
3. The material should be able to support itself structurally.

*Environmental Evaluation of the Woven Screen Memory, Reliability Report TR1-1168, 6 July 1965

The only type of material tested that satisfied all of the above characteristics was silicone rubber. The General Electric RTV-615 material was finally selected because it does have the above characteristics; in addition, it is transparent, facilitating inspection.

The design of the stack has passed through three phases. Each phase resulted from the studies that were being conducted concurrently with the design effort. The three phases were:

1. In the original packaging concept, the planes were interconnected by four circuit boards on the edges of the planes. These boards provided interconnections for the stack and the diode selection matrix, as well as the form for encapsulating the stack. Everything was embedded in a single casting.

   After handling the planes in Librascope's Microelectronics Packaging Laboratory and attempting to interconnect them, it was soon discovered that it is essential to provide for electrical testing of each plane after assembly and for the option of replacing a plane.

2. The second design featured each plane embedded in a "picture frame", again with all leads (both ends of each word coil and both ends of each plated wire) coming out of the casting. These planes could be individually tested and subsequently interconnected in the same manner as the first design.

   Two problems were found:

   a. The "picture frame" required considerably more volume than the original design.

   b. The large number of interconnections crossing boundaries between the encapsulated mat and the frame and again between the frame and the interconnection circuit board was cause for concern for the vibration characteristics of the system.

3. The final design represents a compromise between the repairability and interconnection criteria. In this design two woven plated-wire mats and associated word selection diodes are mounted on either side of an etched epoxy-glass circuit board. Each assembly (or module) contains 64 words 80 bits long with the words connected into two separate 4 x 8 diode-isolated selection matrices. A module can be tested before final assembly and repaired if necessary. The modules can be coupled together to make a stack of almost any proportion.

The stack assembly procedure in Section 5.4 contains a step by step description of the assembly technique that has been demonstrated to be capable of producing a plated wire memory module meeting all environmental requirements. Photographs of the finished breadboard stack and the etched circuit board used in its assembly are shown in figures 4.3-1 and 4.3-2.

4.4 CIRCUIT MODULES

Figure 4.4-1 is a photograph of a typical electronic circuit module. Module circuit boards for iterative circuits use etched wiring while "one-of-a-kind" circuits used hand wired boards. The module header was made by Elco Pacific Corporation to Librascope drawing L 540 001 916. Module covers are standard plastic cups manufactured by Electronics Production and Development Company, part #BC2-2, cut to 1.062 inches in height. The module covers are color coded and have printed initials designating the circuit each contains. A list of circuit symbols is shown in Table 4.4-1.

4.5 FABRICATION

Figure 4.5-1 is a photograph of the back of the breadboard assembly showing wiring. Point to point wiring, utilizing the shortest path, is used to provide good high frequency propagation characteristics. Module layout provides for short, straight paths for critical wiring. Soldered connections are used throughout. Notice the basing arrangement for power distribution. Capacitive filters are provided where needed.

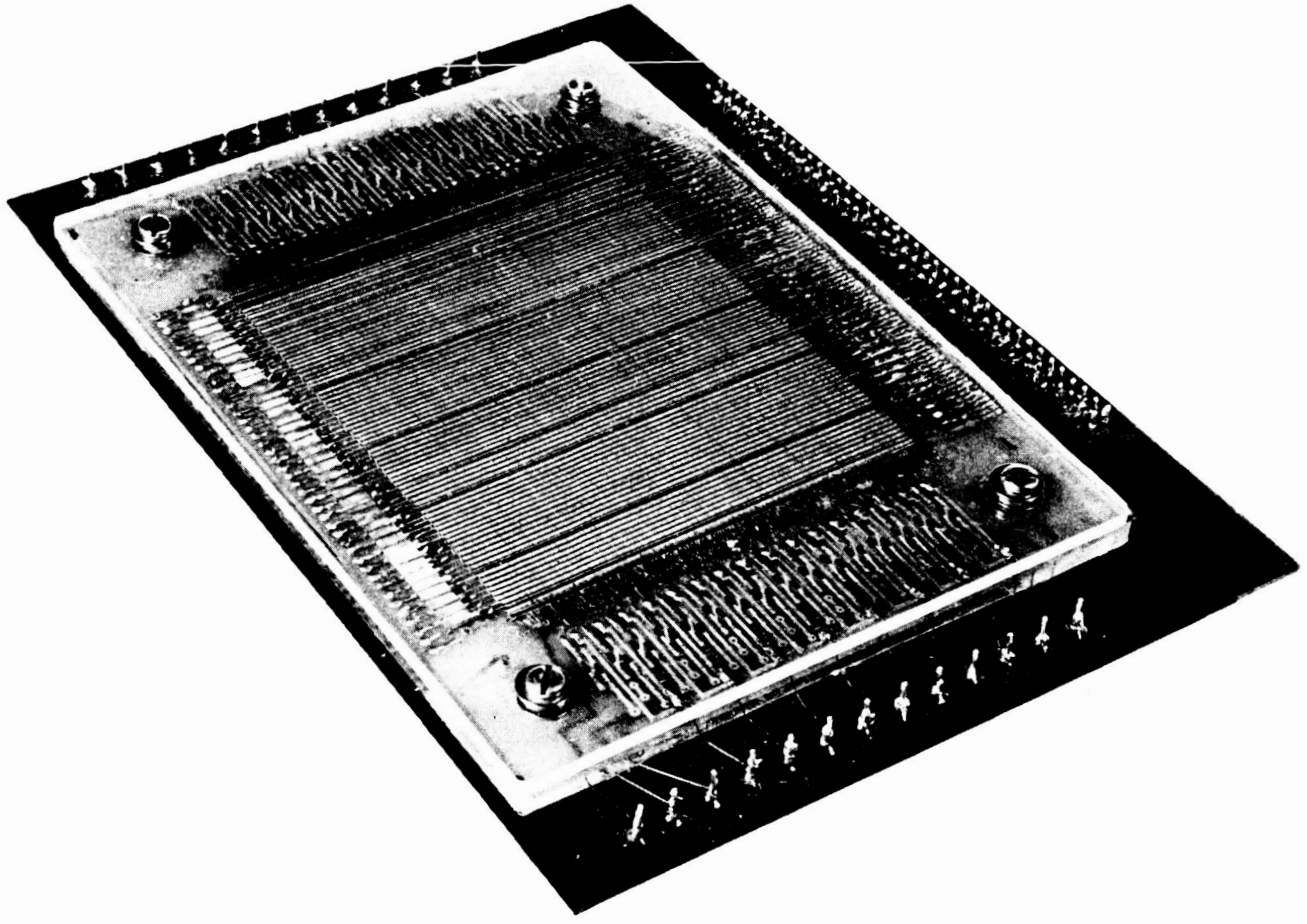


Figure 4.3-1 Encapsulated Breadboard Memory Stack

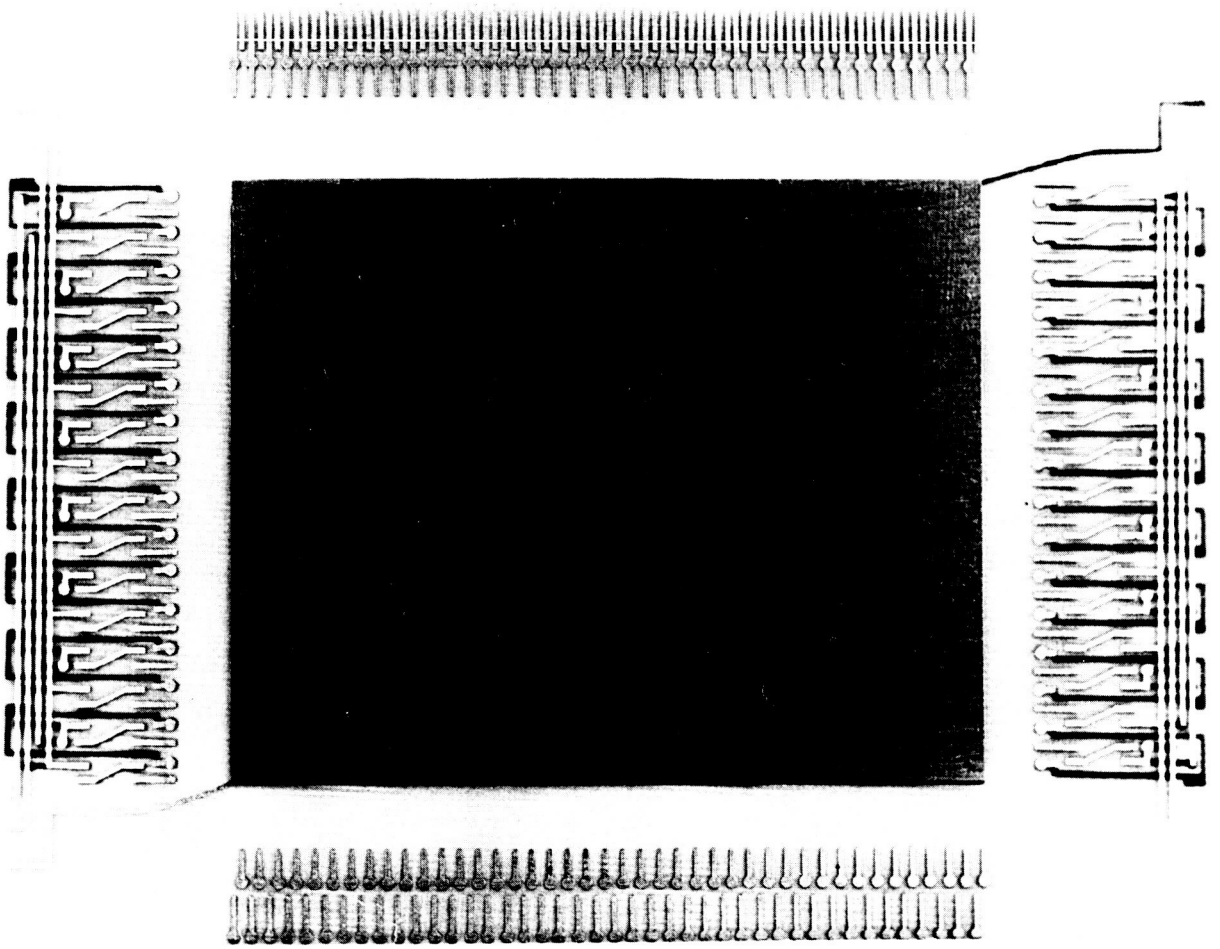


Figure 4.3-2 Circuit Board For Memory Module

Table 4.4-1 Circuit Symbols

ADT	Address Duration Timing Generator
AT	Obsolete - replaced by ADT
BC	Bit Counter
BCC	Bit Counter Control
B01-B16	Bit Counter Stages 1 through 16
CKR	Clock Receiver
CRT	Bit Counter Reset Timing Generator
CSR	Clear Signal Receiver
CT	Obsolete - replaced by CRT
DCD	Obsolete - replaced by DCS
DCS	Digit Current Sink
DD	Digit Driver
DO	Data Output
DS	D Switch
DT	Obsolete - replaced by IDT
DWT	Digit Write Timing Generator
DXF	Digit Transformer
I_D	Digit Current
IDT	Initial Delay Timing Generator
Iw	Word Current
Iww	Word Write Current
MPT	Marker Pulse Timing Generator
MT	Obsolete - replaced by MPT
M01 - M16	Marker output circuits1 - 16
RA	Read Amplifier
RT	Obsolete - replaced by WCT
RWC	Read-Write Control
RXF	Read Transformer Circuit

Table 4.4-1 Circuit Symbols - Continued

SN	Read Amplifier Shaping Network
TG	Timing Generator
TN	Timing Network
Vo	Output voltage for sensing from memory plane
WCD	Word current driver - same as WPG - word pulse generator, which is preferred
WCT	Word Current Timing Generator
WPG	Word Pulse Generator
WS	Word Switch
WSA	Word Switch, A axis
WSB	Word Switch, B axis
WT	Obsolete - replaced by DWT

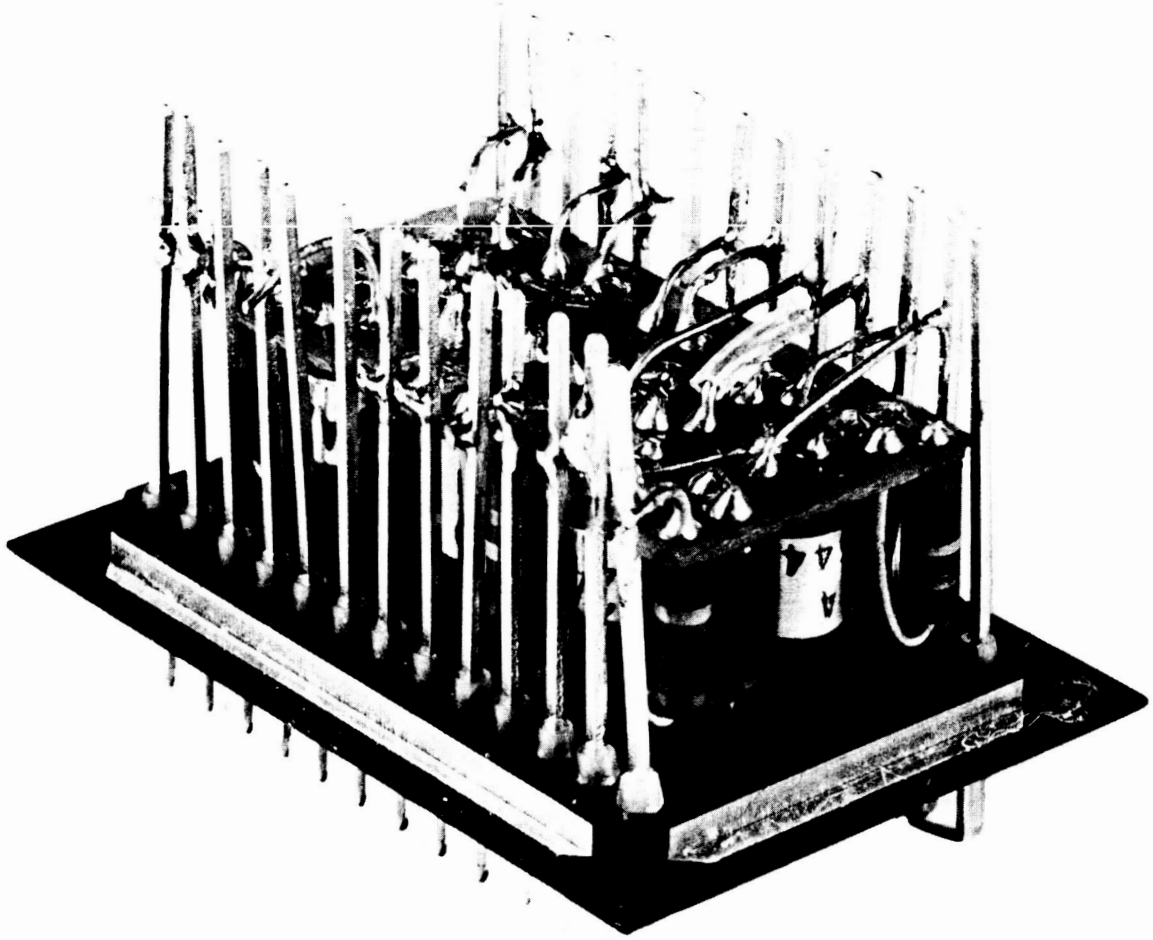


Figure 4.4-1 Typical Breadboard Circuit Module

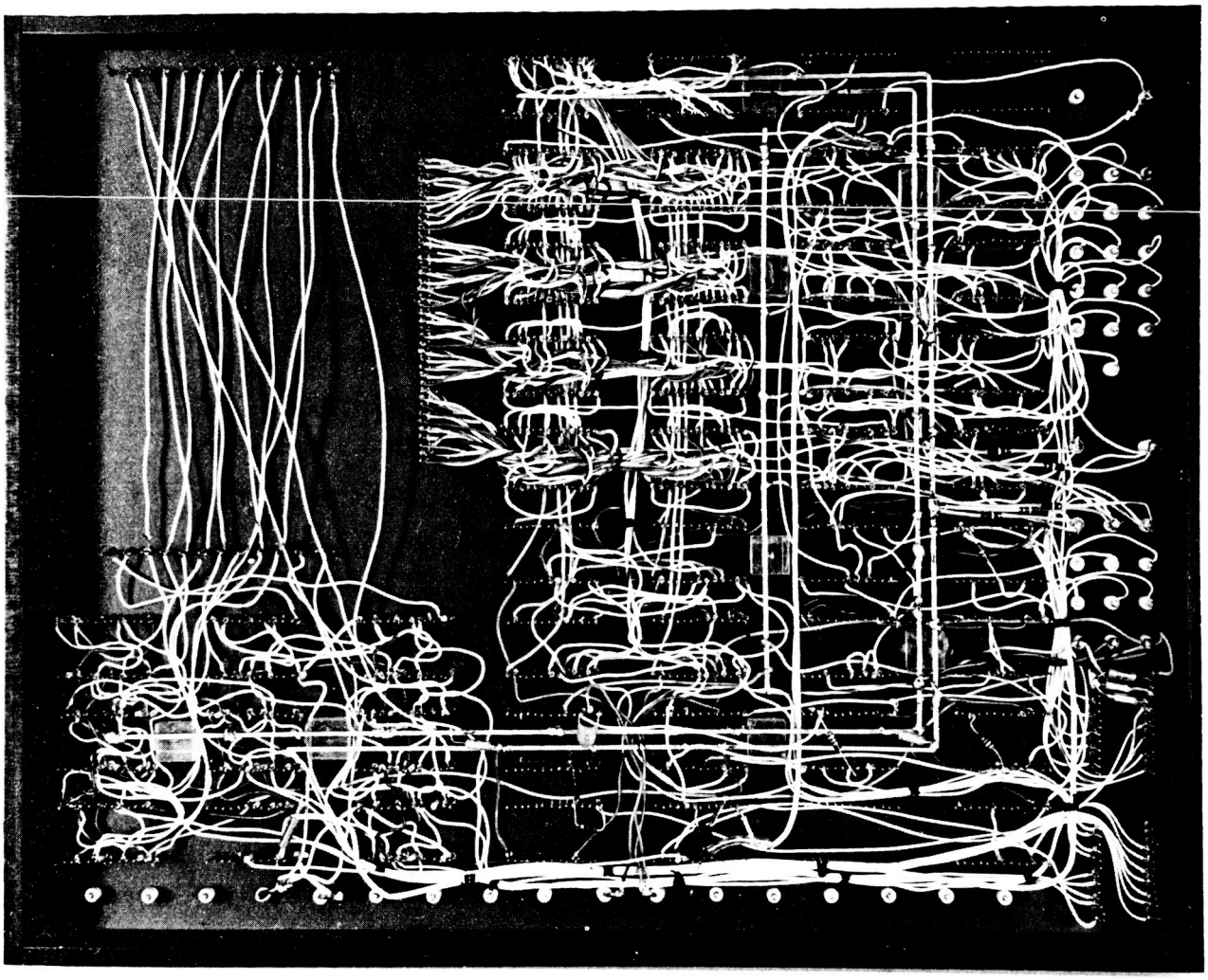


Figure 4.5-1 Breadboard Chassis Wiring

Section 5

PROTOTYPE PACKAGING STUDY

5.1 INTRODUCTION AND SCOPE OF TASK

This section of the report describes the design study effort to develop the feasibility of expanding and repackaging the breadboard system into a pre-production prototype of a qualified JPL low power space memory. The prototype Memory System Package is shown in figure 5.1-1. The prototype design was constrained by the following priorities, in descending order:

1. high reliability
2. low system volume
3. circuit isolation
4. repairability
5. cost
6. low system weight

As originally proposed, the system utilized monolithic and hybrid integrated circuits in the electronics modules with a total system volume of 30.0 cubic inches. In the interest of enhanced reliability, the hybrid integrated circuits were replaced by discrete components and monolithic integrated circuits packaged in cordwood modules. The cordwood modules were then packaged onto two circuit boards, Digit and Word Electronics Modules. This change to discrete components resulted in a system volume increase from the original 30 cubic inches, to a final total of 48 cubic inches.

The study involved system organization from a packaging view point, the use of standard cordwood modules and interconnect techniques, arrangement of circuits to simplify interconnections, manufacturability and maintenance.

In addition, discussions on material selection and environmental conditions are included. A structural and thermal analysis was accomplished to define the environmental limits of the final system package.

Under the System Mechanical Configuration Section (Section 5.2) several alternate design concepts are described, with the relative advantages and disadvantages of each.

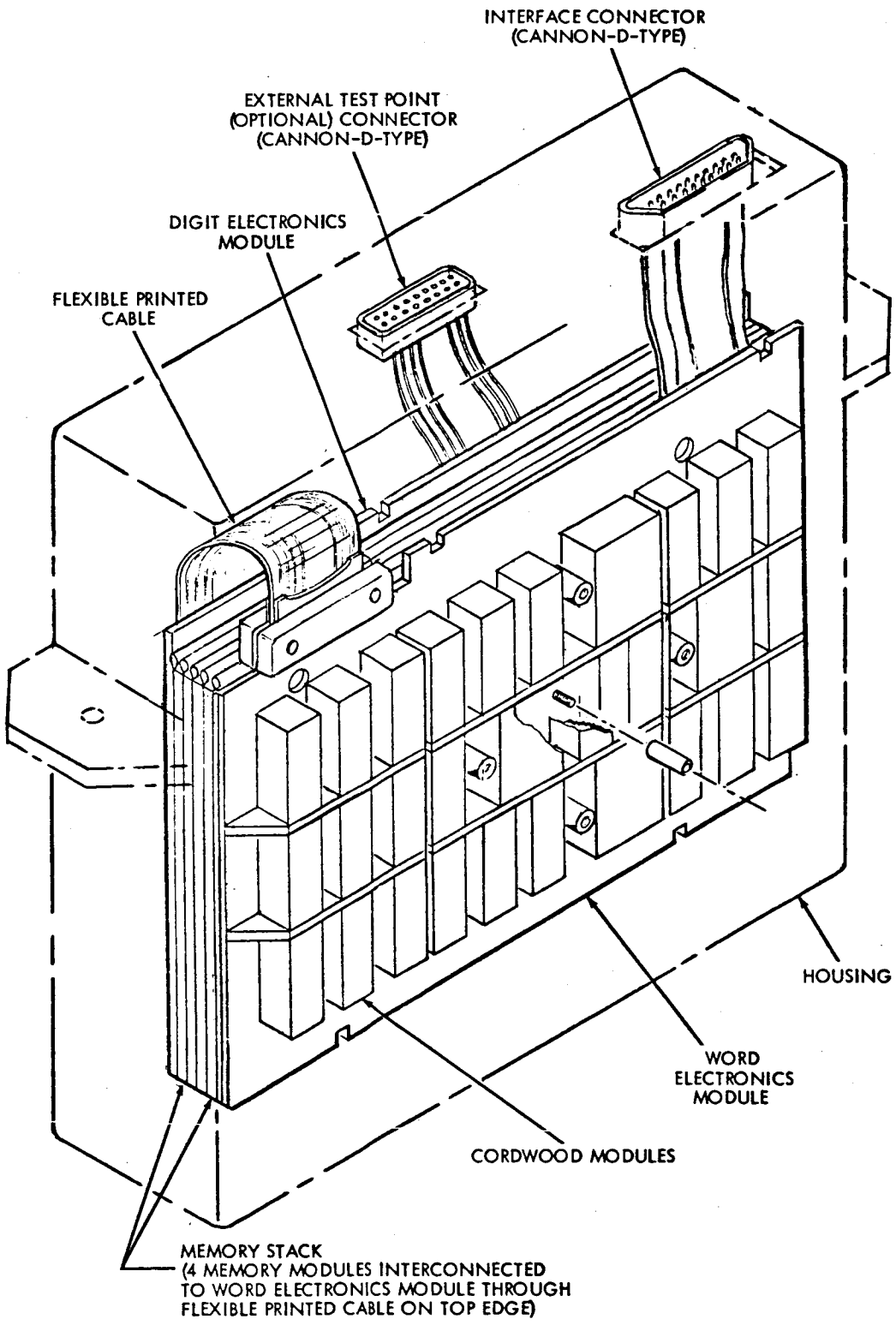


Figure 5.1-1 Prototype Memory System Package

5.1.1 Definition of Terms

The following is a list of terms and definitions used in describing the memory package.

SYSTEM	Low Power Space Memory
MEMORY:	System
HOUSING:	Metal environmental cover
MODULE:	Matrix assembly with a group of cordwood modules, or a group of memory mats.
STACK:	Interconnected assembly of four (4) memory modules.
MATRIX:	Printed circuit (single or double sided) interconnect system for groups of cordwood modules, or woven plated memory mats.
CORDWOOD MODULE:	Sub-module, sub-circuit
INTRACONNECT:	Permanent electrical connection internal to an encapsulated module.
INTERCONNECT:	Permanent electrical connection external to any encapsulated or potted module.
WPWM MAT:	Woven plated wire fabric as taken from the loom.
ENCAPSULATE:	Plastic covering for an independent, completed circuit or sub-circuit. Embedding an electrical assembly in a case or shell which remains an integral part of the unit. Potting, brush application of epoxies, freeze-coating, etc.
FEED-THROUGH:	Electrical jumper from header to header of a cordwood module.
HEADER:	Printed circuit used to interconnect circuit elements on cordwood modules.

PLANE: Assembly consisting of mat and Printed Circuit matrix.

DIGIT WIRE: A component part of the mat, whether plated or dummy.

CONSTRUCTION WIRE: Heavy wire before and after digit wires for holding mat shape.

5.1.2 Standards and Specifications

The following specifications and standards were used as guides in the work done for the Prototype Packaging Study.

JPL 30250B: Environmental Spec., Mariner C Flight Equip., Type Approval Environmental Test Procedures, Assembly Level.

JPL VOL-505-ETS: Environmental Spec., Voyager Capsule Flight Equip. Heat Sterilization and Ethylene Oxide Decontamination environments

JPL 31252: General Spec., Mariner C Equipment. Minimum Magnetic field

JPL ZPP-2061-PPL-E: JPL Preferred Parts List

JPL Contract No. 950986. Exhibit I determines the extent of applicability of all specifications and standards.

Librascope specification: No. L180 000 587, Printed Circuit Design and Fabrication.

5.2 SYSTEM MECHANICAL CONFIGURATION

5.2.1 System Description

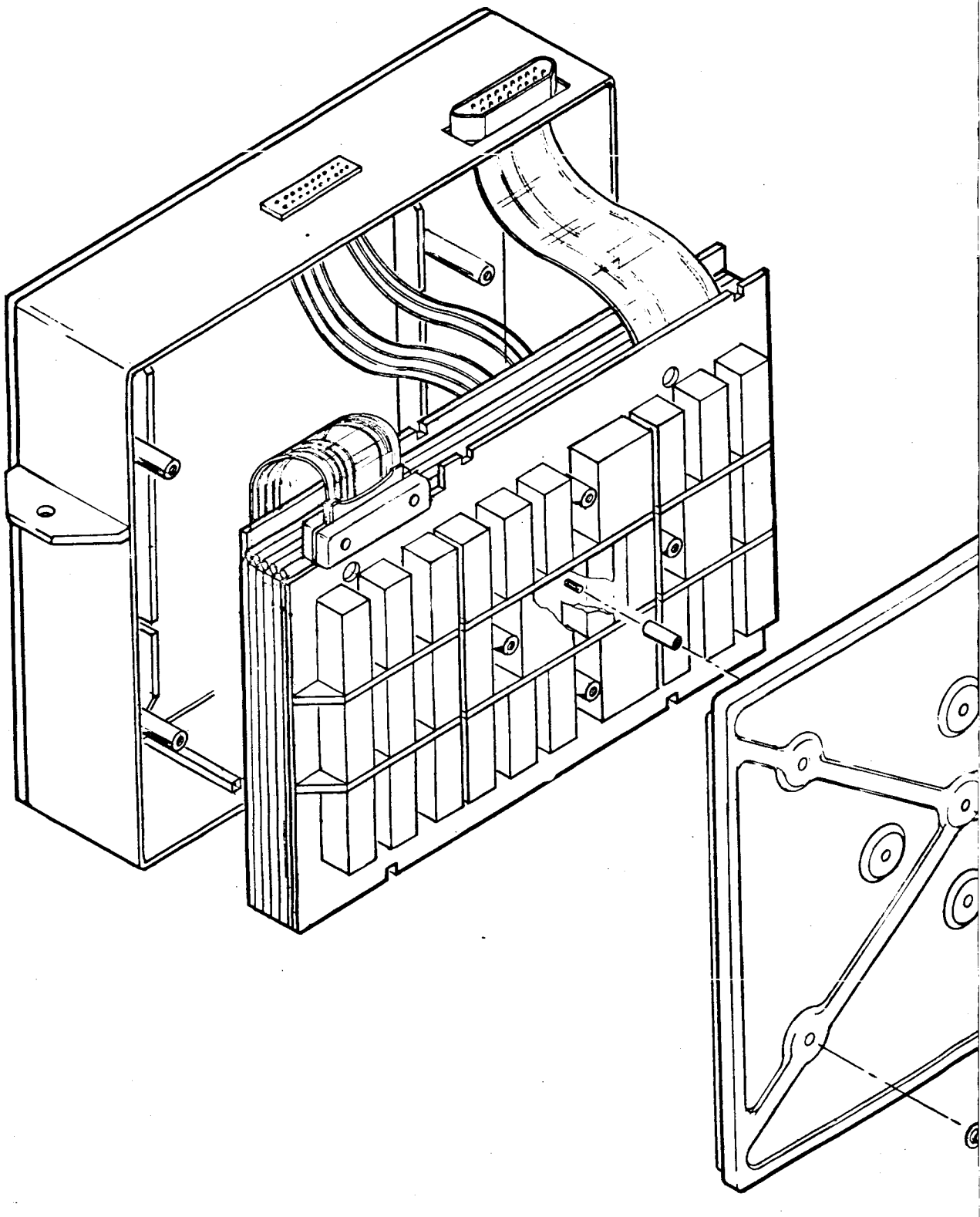
The memory system consists of

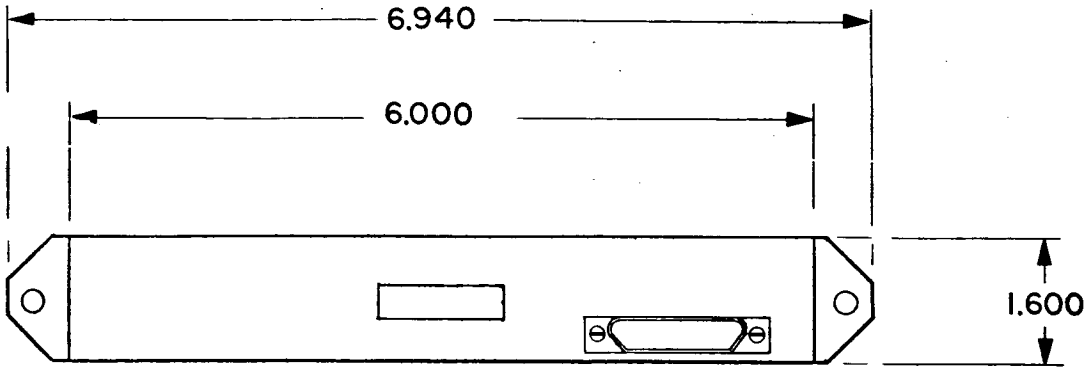
(1) Word Electronics Module
(1) Digit Electronics Module
(4) Memory Modules
(1) Cast Aluminum Housing with end covers

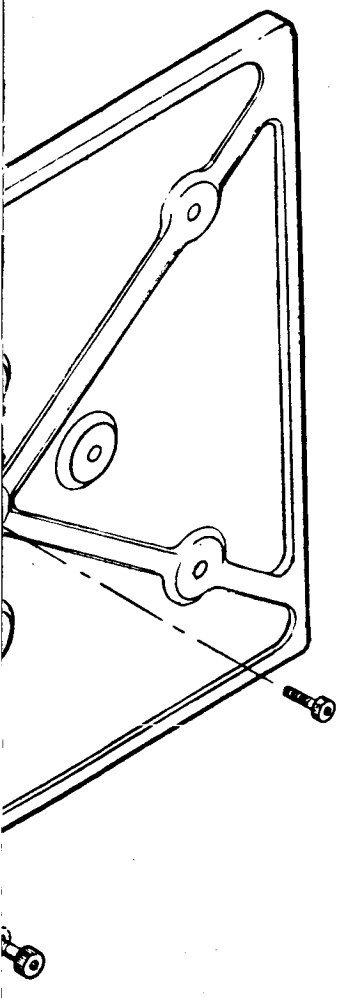
The modular construction technique is proposed for maximum volume reduction with conventional components, improved reliability, orderliness of design and manufacturability. (See figures 5.2-1 and 5.2-2.)

Both sides of each module are encapsulated in RTV 615 Silicone rubber. The inside surface of each end cover is similarly coated. The rear cover has four (4) studs that extend through the housing, and act as support for the modules. Thus, when the six (6) modules are suspended from the rear cover studs and the front cover is fastened to these studs, the entire assembly is compressed by a controlled force; which is a function of the torque applied to the four (4) fasteners. The compressive force must be a repeatable constant in order to preserve the validity of environmental test data. Precision is ensured by the stepped inner surface of the covers. As torque is applied the covers bottom against the housing, providing three dimensional registration.

A breakdown of the electrical schematics to minimize the number of repeatable sub-circuits simplified the system interconnection design. The basic element is the cordwood module, which is a soldered, and plastic embedded unit. Groups of cordwood modules are interconnected to make up the module assembly. The use of flexible cables facilitates maintainability and simplified servicing techniques, in addition to miniaturization. The use of friction connectors is kept to a minimum, since friction connectors are known to be less reliable than solid connections. Prewiring, such as printed circuits and matrix techniques, reduces the possibility of manufacturing error and improves manufacturing efficiency.







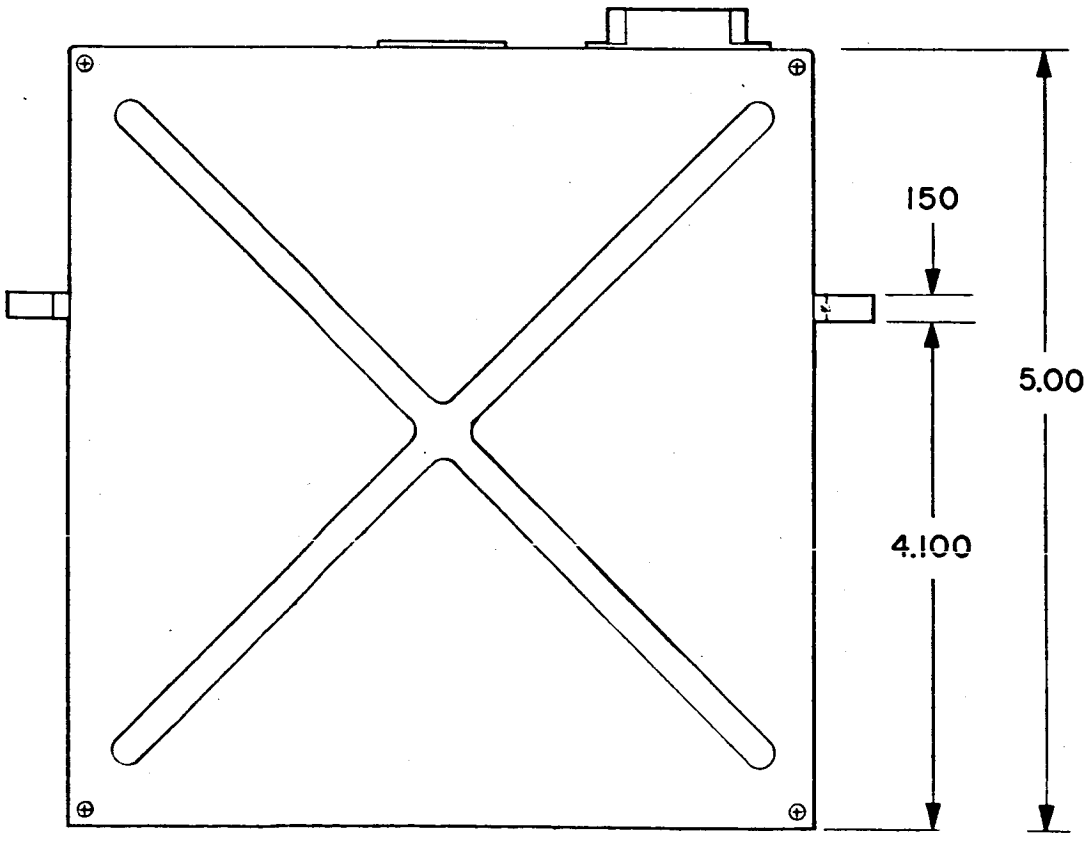


Figure 5.2-1 System Assembly

[redacted]

17°

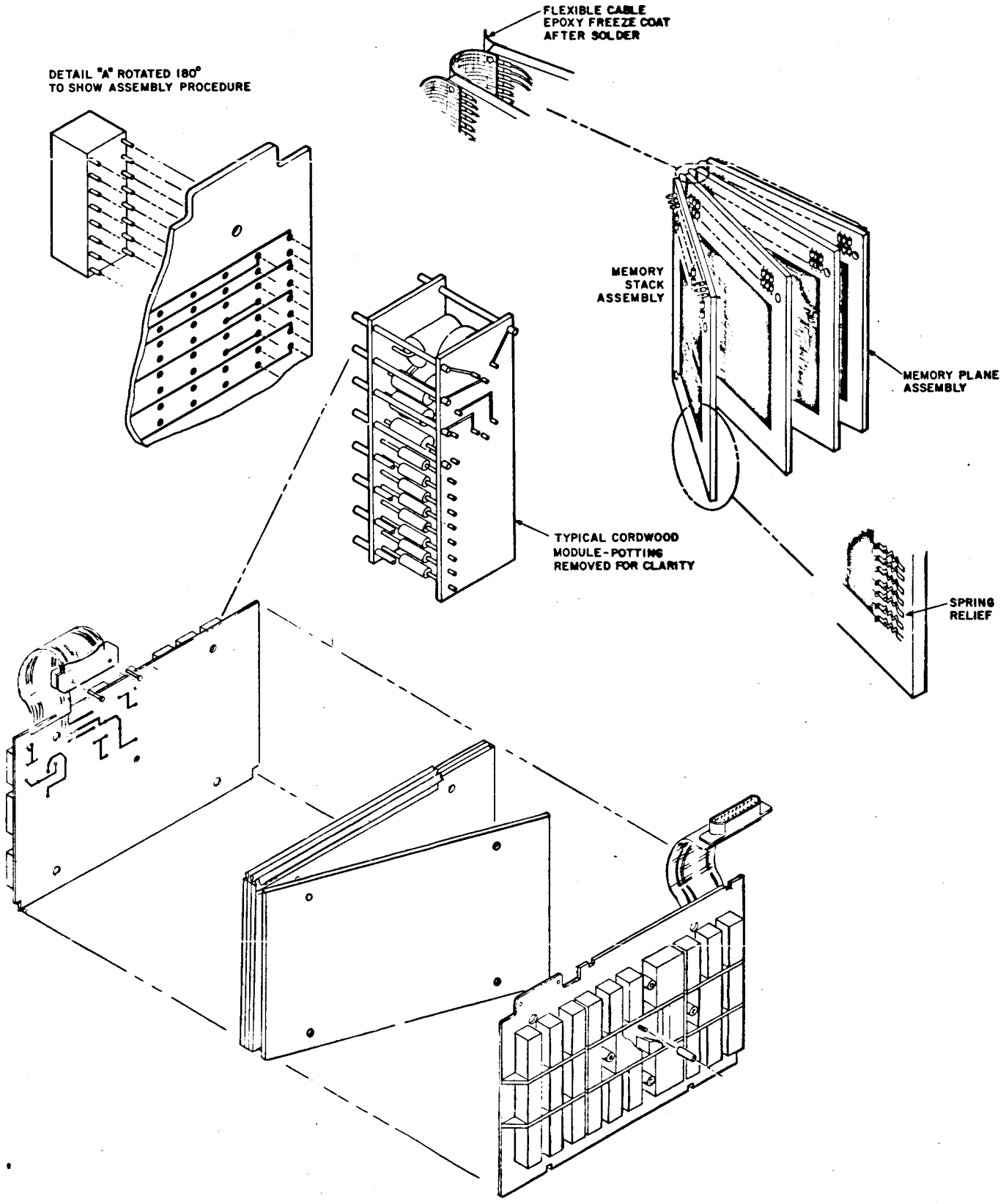


Figure 5.2-2 Module Assembly and Details

Communication from the digit electronics module to the word electronics module is made through flexible cable and a printed circuit edge connector. Communication to the memory stack module is made through flexible cables, solder connected at each end.

All external lines originate on the word electronics module and terminate in a Cannon "D" type connector mounted to the system housing. A second Cannon "D" connector may be provided as shown in Figures 5.2-1 and 5.2-2 to make test points externally accessible, if required.

The potting material used on the stack and modules will seal the electronics, a system seal is not necessary.

5.2.2 System Weight and Volume

Listed below are the calculated constituent weights of the proposed system. The final prototype system will closely approximate these values.

All cordwood modules at avg. weight 0.035 lb x 54	= 1.89 lbs.
Memory Plane Assy. at approximately 0.153 x 4	= 0.61 lbs.
Housing and end covers (alum at approx. 0.1 lbs/in^3)	= 0.81 lbs.
Encapsulating (RTV 615) material	= 0.12 lbs.
Connectors, Cables, Fasteners	0.60 lbs.
Total System Weight	4.03 lbs.

As shown in Figure 5.2-1 the overall envelope of the system (excluding mounting ears) is 5.00 high x 6.000 wide x 1.600 deep = 48.00 in^3 total volume.

These overall dimensions meet the subchassis outline requirements of JPL drawing 4901045, with standard width as defined in JPL drawing D4901049. The length and height dimensions pose no problems. Four representative cordwood module types (of 12 total types in system) were completely designed to established layout and sizing data. (See figures 5.3-1 through 5.3-5 in Section 5.3)

Since these (4) module types represent approximately 50% of the total module count in the system, it appears quite certain that the width dimension will present no difficulty either.

The cordwood density on the Digit Electronics Module is approaching its maximum in the present design stage. If expansion in this area should prove necessary in the final design, some of the functions could be moved to the low density Word Electronics Module. However, extrapolation of present sizing data indicates that this will not be necessary.

Detailed sizing data for the electronics and memory modules is presented in following sections.

5.2.3 Original JPL Proposal Packaging Concept vs. Proposed Final Design

The memory system packaging concept delineated in Figures 5.2-3, 5.2-4, and 5.2-5 was the preliminary concept proposed to JPL, as the basis for this prototype packaging study contract. This concept served as the starting point for all other configurations considered, including the sampling of alternate designs shown below, and the final design proposed in this report.

The originally proposed package utilized Integrated Circuits to the maximum extent practicable, including hybrids. Librascope was dissuaded from the use of hybrids during subsequent discussions with JPL engineers, due to the lack of reliability data. When the decision to use cordwood modules was reached, an attempt was made to hold the originally proposed volume of 30 cubic inches. This effort led to several hard-wired concepts, one of which is shown below. A hard-wired package is inherently difficult to check-out, repair and maintain. These problems proved severe, and other approaches using module connectors were investigated. Here, volumetric increases became intolerable, and the final configuration evolved as engineering trade-offs were made. In the final design, reliability was increased, maintainability was not compromised, but a weight increase was necessary and the volume was increased from 30 to 48 cubic inches.

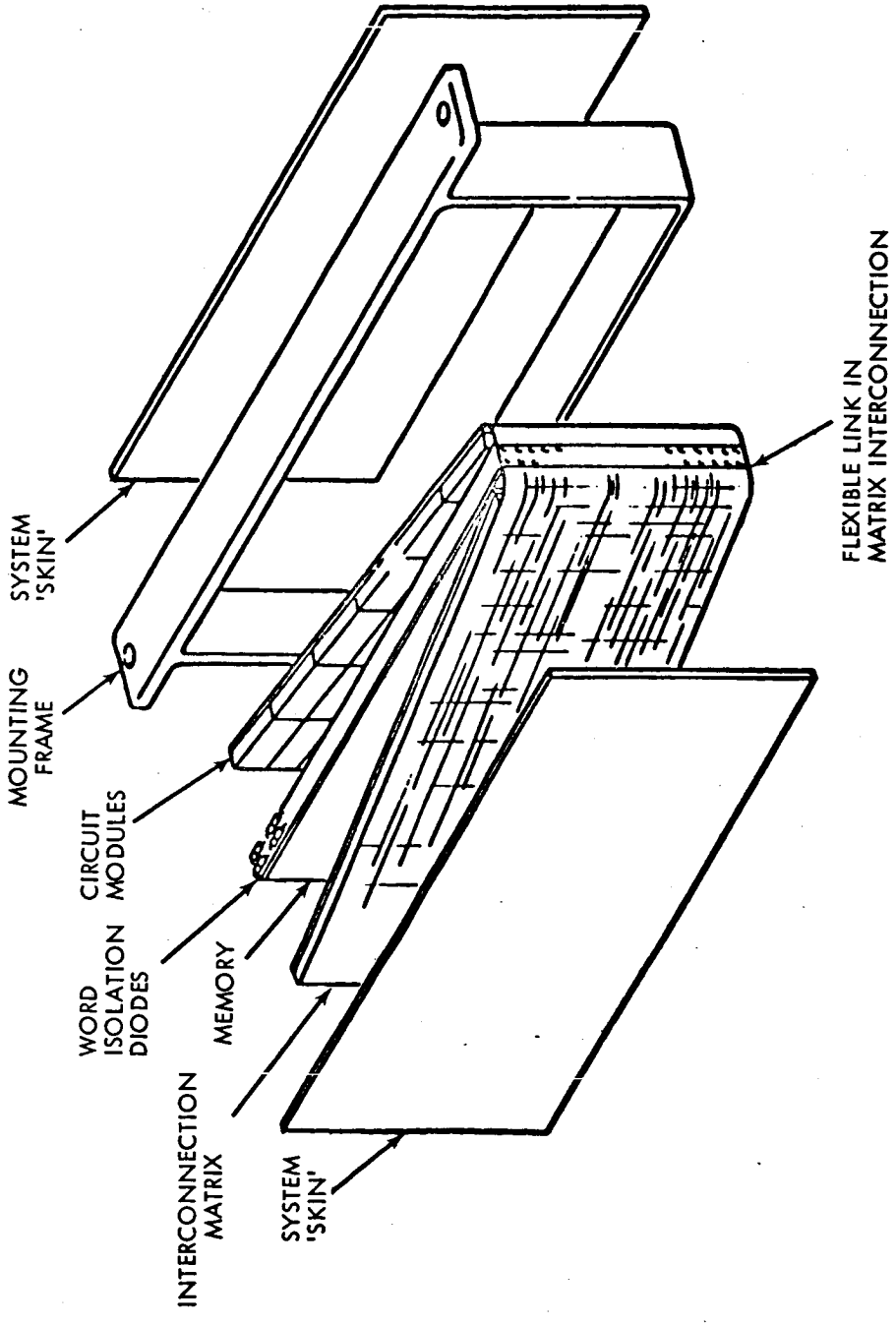


Figure 5.2-3 Alternate Packaging Concept
(Original Proposal Concept)

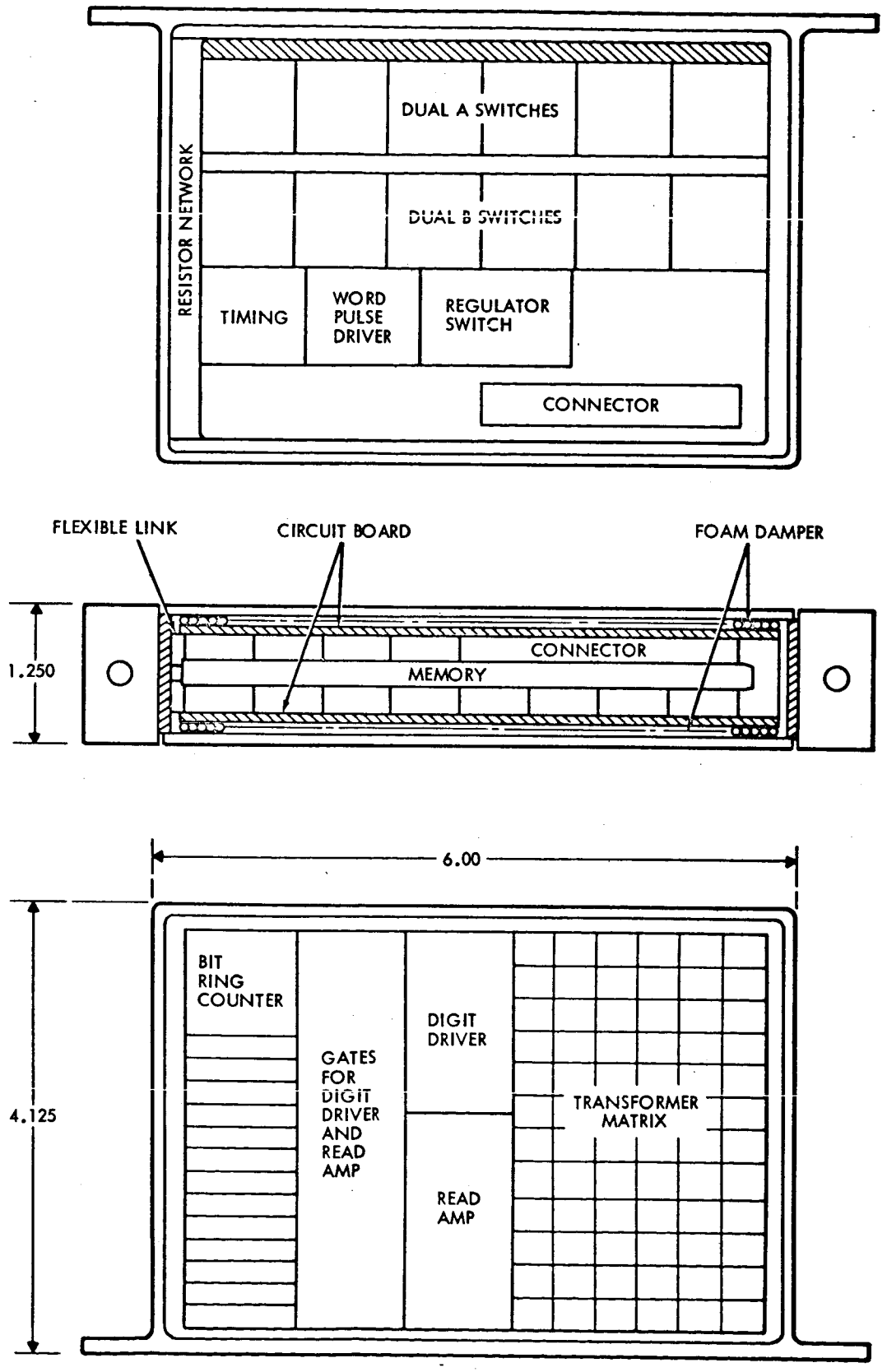


Figure 5.2-4 Alternate Packaging Concept
(Original Proposal Concept)

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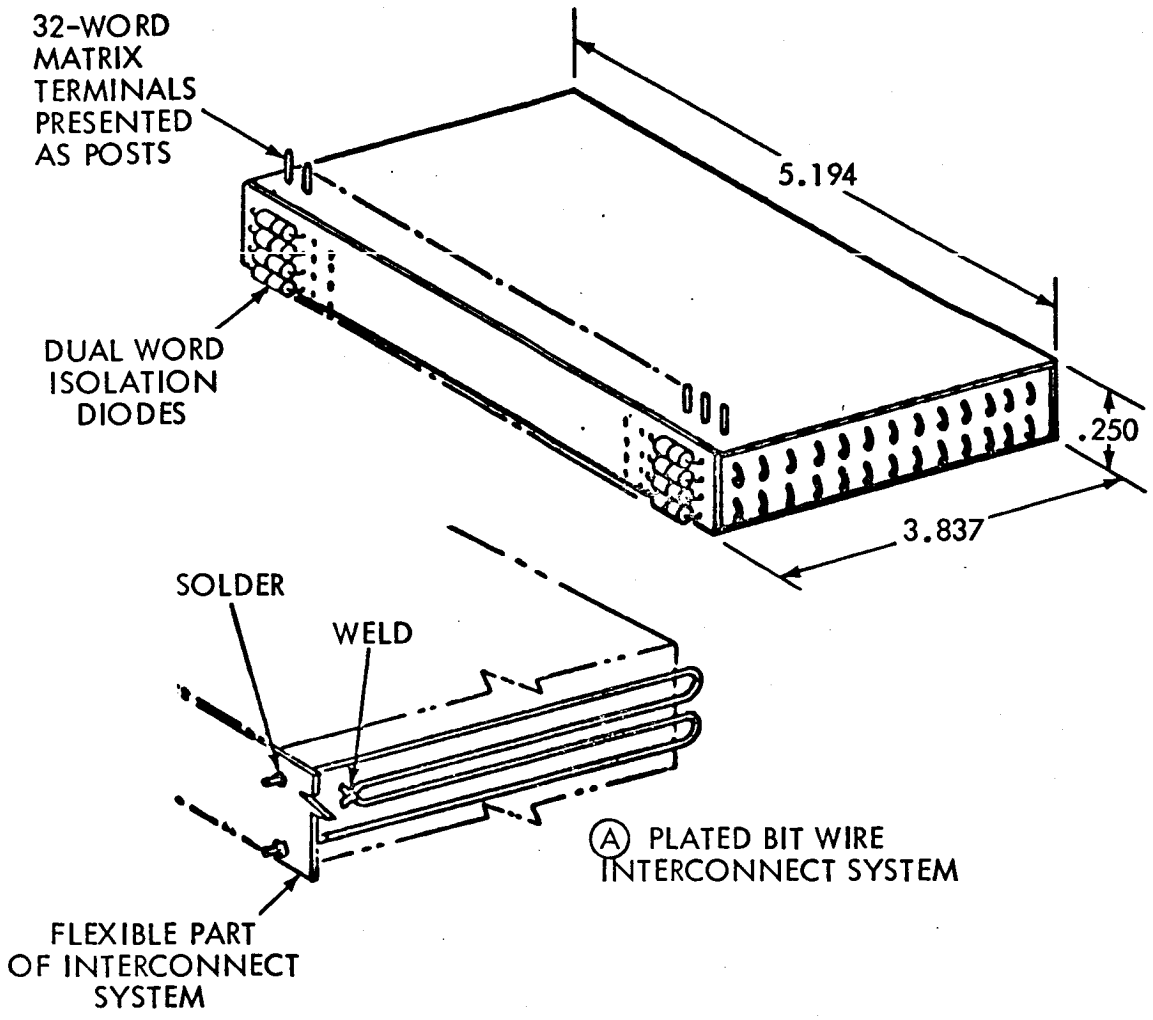
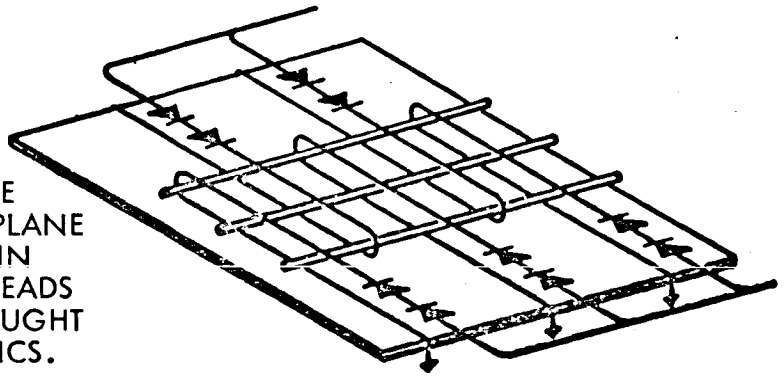




THE DIODE ENDS OF THE 64-WORD LINES ON A PLANE ARE BUSSED TOGETHER IN GROUPS OF 16 AND 4 LEADS FROM EACH PLANE BROUGHT OUT TO THE ELECTRONICS.

THE RETURN ENDS ARE BUSSED VERTICALLY THRU THE STACK SUCH THAT THE FIRST WORD IN EACH OF THE 4 GROUPS OF 16 HAVE A COMMON RETURN

Figure 5.2-5 Alternate Packaging Concept
(Original Proposal Concept)

5.2.4 Alternate Package Designs Considered

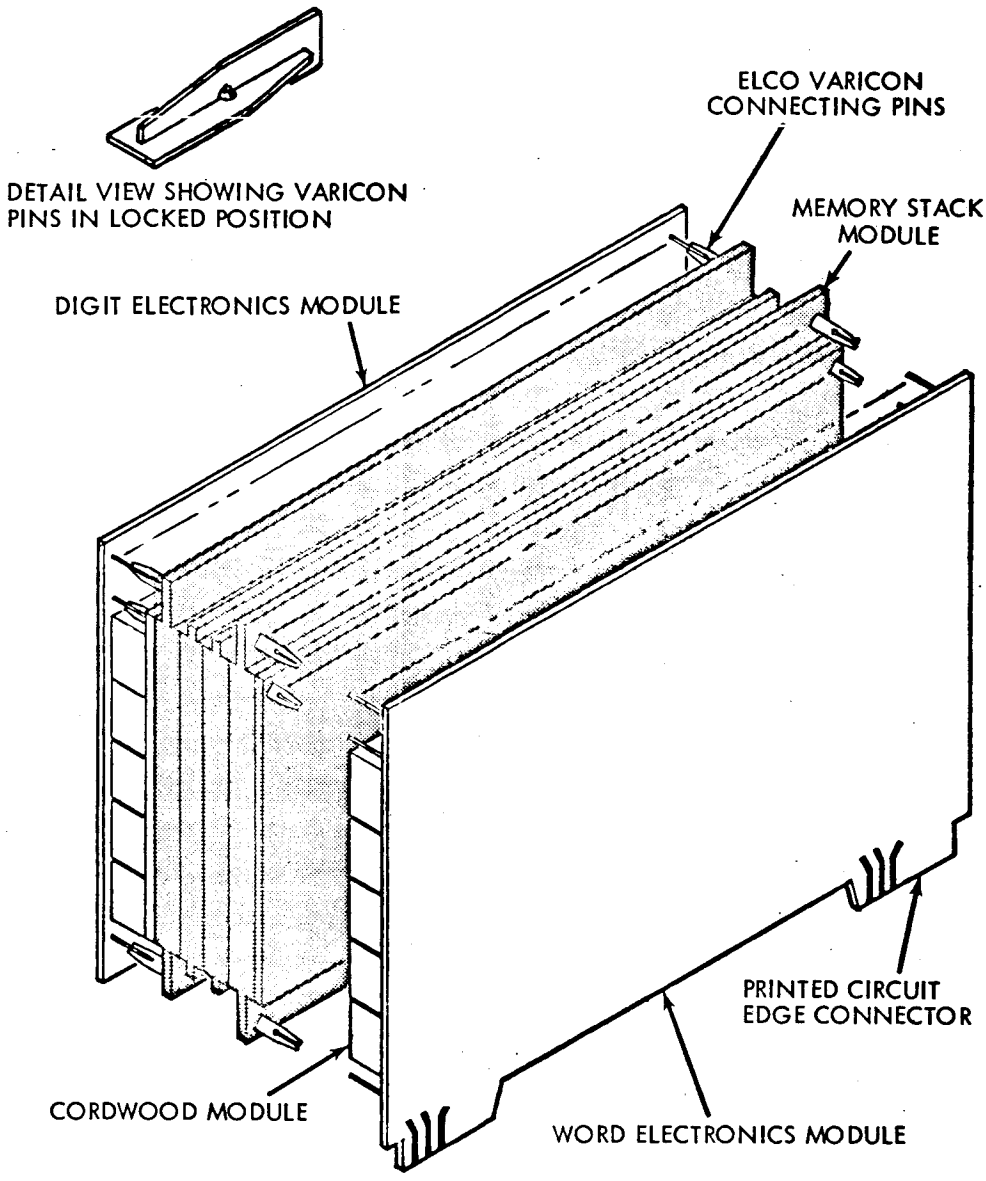
The proposed prototype package design is the final refinement of many possible concepts investigated. In addition to the large number of overall package concepts considered, a thorough analysis of attendant design detail problems was performed. Such matters as structural de-coupling of stresses, maintenance techniques, functional organization, solder, weld, and encapsulation processes, etc. were assembled, reviewed and isolated prior to making decisions bearing an optimum engineering trade-offs.

A representative sampling of some of the concepts investigated is given below with a brief discussion of the salient advantages and disadvantages of each.

5.2.4.1 System Assembly Through Connector Pins. A package concept was considered utilizing Elco Varicon connecting pins for all inter-module connections. See Figure 5.2-6 for the system concept and Figure 5.2-7 for a view of an individual module. The vertically oriented connector pins would mate with a connector to the external interface, the horizontal pins interconnect all modules.

The major advantage of this approach is in maintenance and repair. The system can be completely disassembled by unplugging each board. Check-out and trouble-shooting could be expedited by exchanging modules to accelerate fault isolation. Since inter-module connections are made through solid pins; fatigue, overstressing, shock and vibration problems in module interconnect cables are alleviated. Although the Elco pins rely on friction for contact integrity, they can meet high reliability requirements in vibration and shock environments.

Some of the disadvantages of the connector pin approach are as follows: The cumulative pin retention force on a given module would require excessive force to separate modules. This force, applied to either electronics or memory modules, might overstress the boards causing conductor path or component damage. Consideration was given to various



Alternate (Rejected) Packaging Concept
All module interconnects made through Varicon friction locked connector pins. (See figure 5.2-7 for view of individual module)

Figure 5.2-6 Alternate Packaging Concept

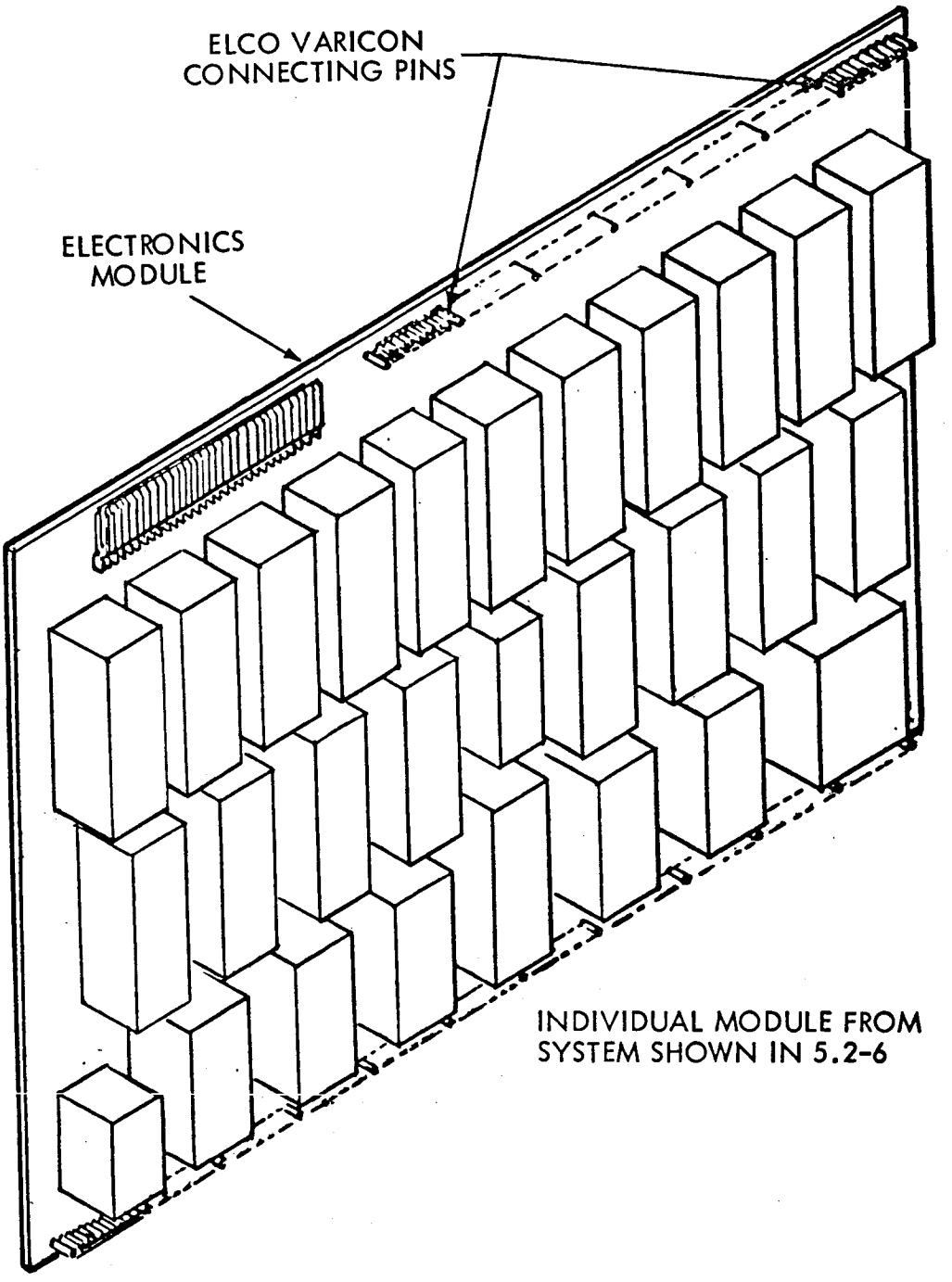


Figure 5.2-7 Alternate Packaging Concept

extraction devices (jacking screws, etc.), but the separating force would have to be distributed over all, or most, of the pins. These remedies add weight and complexity. Another problem arises with pin location tolerances. As mentioned above, these pins can meet high-reliability requirements, but misalignment compromises this capability. Bent pins are another potential problem area.

5.2.4.2 Plug-In Module Nest Concept. Figure 5.2-8 shows a package concept with the external housing serving as a module nest (card cage). The memory matrices and electronics are mounted on removable, plug-in modules. All wiring between modules is done below the connectors, affording ready access.

This method would simplify assembly, checkout and maintenance since all modules are replaceable. As with the Varicon connector pin approach, trouble-shooting is expedited since modules can be substituted to accelerate fault isolation. Individual modules could be checked out in the system by using a point-to-point board extender.

Among the disadvantages is the loss of high-density packing, since clearance must be left between modules for insertion and removal. Also, available printed circuit card connectors are relatively large, and add weight. The relative advantages and disadvantages of this plug-in module concept are essentially similar to those cited above in the Varicon connector pin approach.

5.2.4.3 Encapsulated Hard-Wired Module Concept. The modules shown in Figure 5.2-9 contain both memory and word and digit electronics. Leads from each module protrude from the encapsulated block. The leads pass through printed circuit headers and can be soldered or welded, automatically or manually, to form the inter-module connections. A short, flexible printed circuit cable could be connected to the appropriate pins to form the external interface. The entire package could then be encapsulated forming a simple rugged package with only a cable extending out of the block.

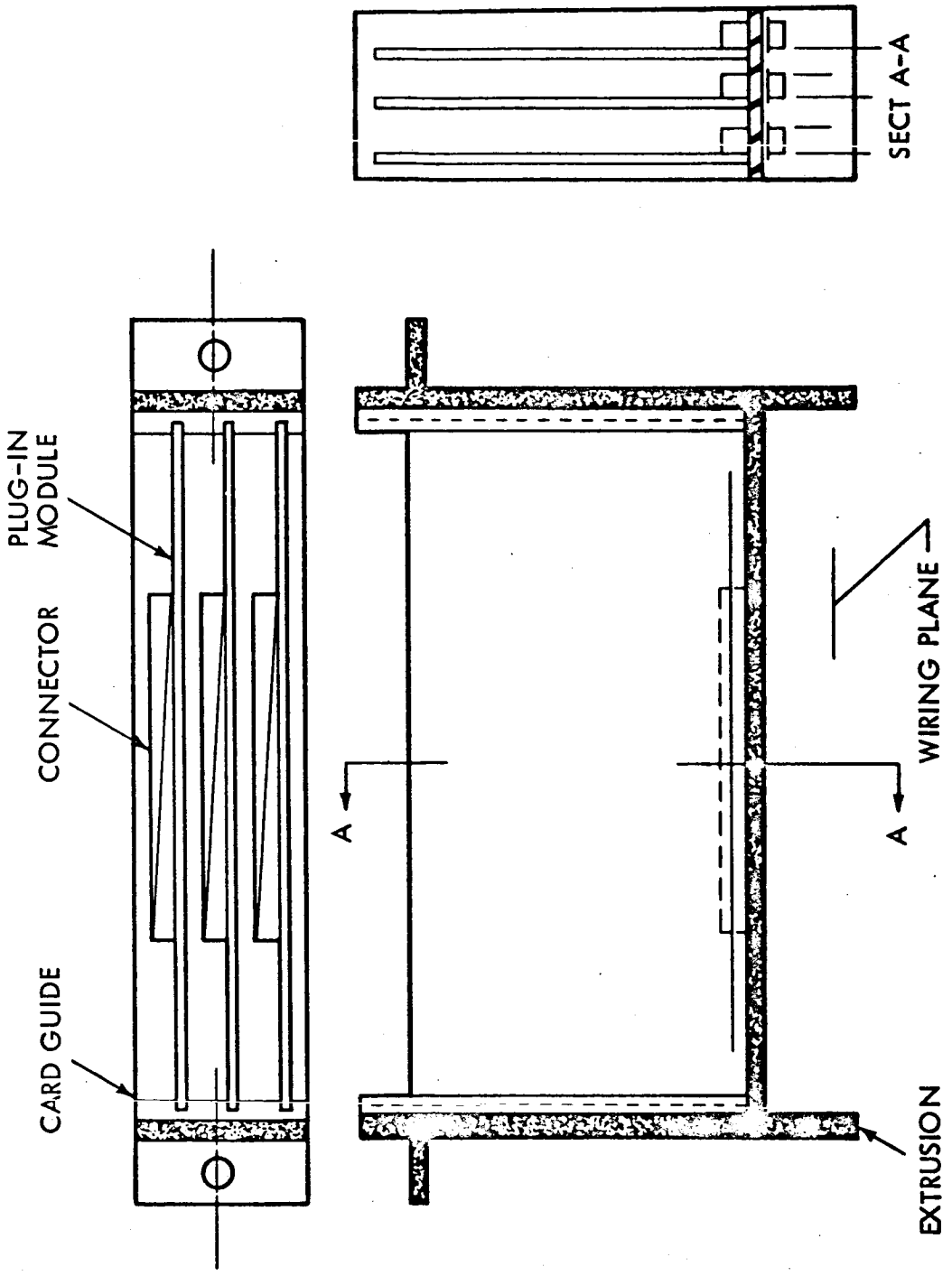


Figure 5.2-8 Alternate Packaging Concept
(frame is module nest with plug-in connectors)

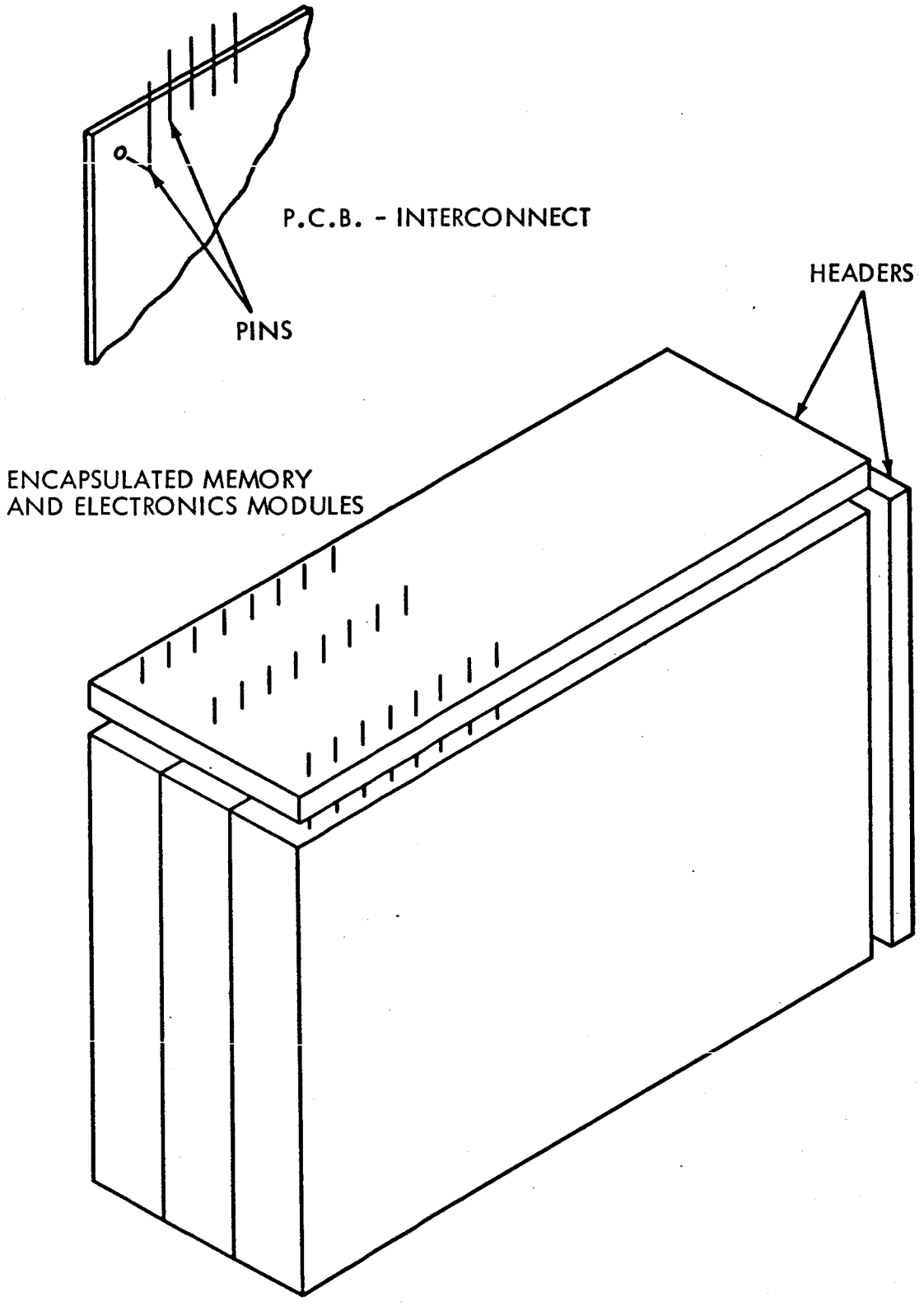


Figure 5.2-9 Alternate Packaging Concept
(Point-to-Point Hard Wired)

The advantages of this concept are ruggedness, reliability and simplicity of design. High stress environments were not considered, but the package could be sheathed in a suitable impact case to distribute loading forces over a maximum surface area. This system would be impervious to intermittent contact problems and fatigue of cables and leads.

The disadvantage, of course, is inability to service the modules. Even replacement of a module would be problematical.

5.2.4.4 Slip-On Light Weight Housing Concept. Many housing configurations were considered before deciding on the proposed prototype design. Earlier concepts were not influenced by high shock load requirements which were added later. Figure 5.2-10 shows a simple yet compact and functional housing.

Removal of a few screws affords access to the entire package. The inter-module connections are similar to those proposed in the prototype. The housing is light-weight and adds little volume to the overall package.

The light weight housing is structurally inadequate for space-borne applications. If hard-impact loads are not to be encountered however, the weight and cost advantages of this approach should be reevaluated.

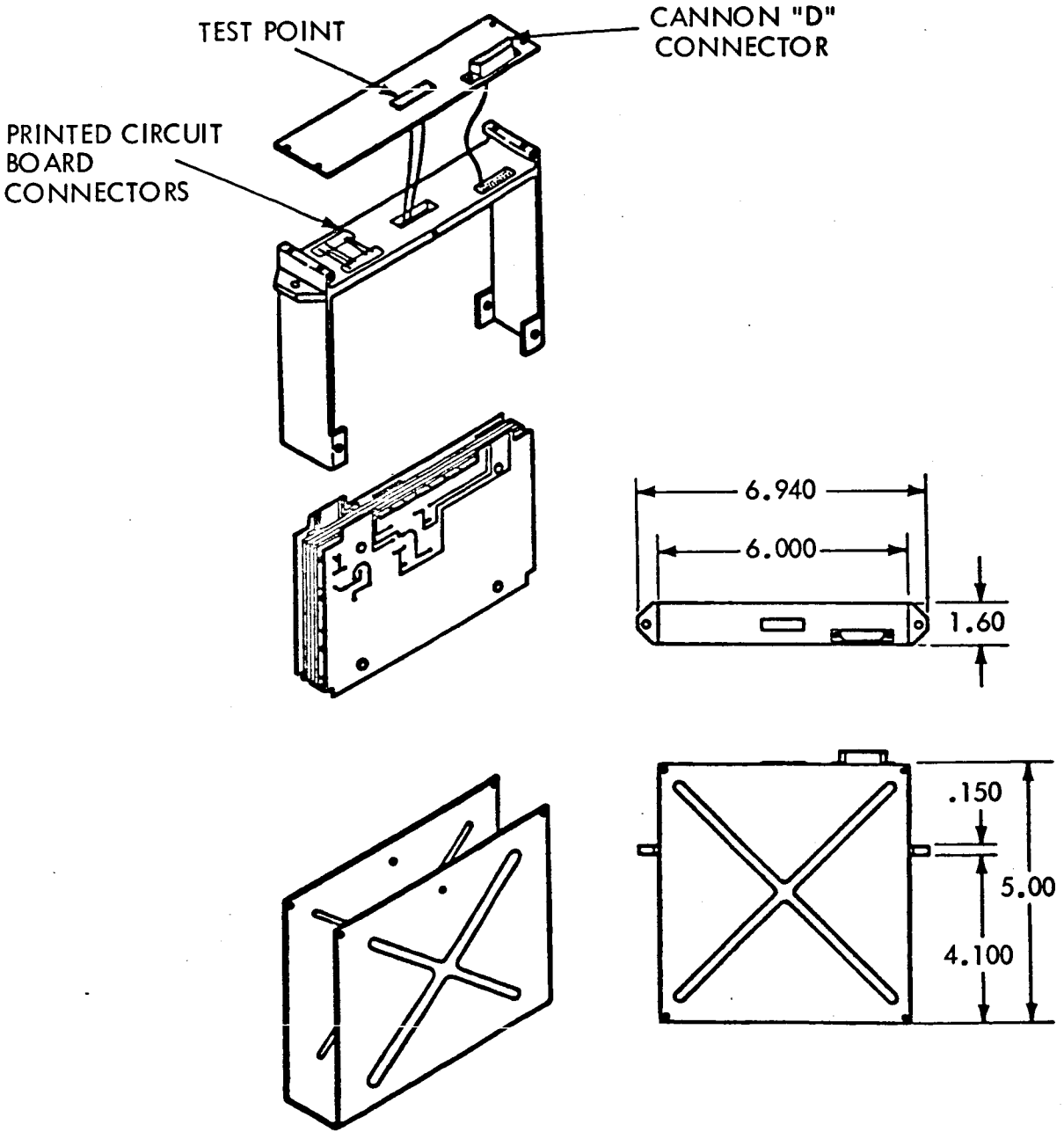


Figure 5.2-10 Alternate Packaging Concept
(Slip-on Lightweight Housing)

5.3 DIGIT AND WORD ELECTRONIC MODULES

The interconnect matrix for the word electronics module and the digit electronics module will be double sided, rib reinforced printed circuit boards, using plated through holes for surface to surface communication. Material will be copper clad per the military specifications noted. The matrix and cordwood module concept was selected for reliability, manufacturability, repairability, heat dissipation, volume and weight reduction, design flexibility, cost and component availability. Once the decision was made to abandon hybrid circuits in favor of discrete components and monolithic integrated circuits, cordwood assemblies became a necessity to hold down system volume.

To verify envelope dimensions and circuit interconnections, it was necessary to completely lay out certain representative cordwood modules. See Figure 5.3-1 through 5.3-4. An enlarged view of a typical cordwood assembly is shown in Figure 5.3-5. Figure 5.3-6 shows techinques for loading components into the cordwood stack.

Circuit isolation between digit and word electronics is maintained by locating the Memory Stack assembly between the high and low level Electronics Modules. Interconnections between the Digit and Word Electronics will be through a printed circuit type connector. All leads are the shortest length possible within the limits of the latest state-of-the-art. Additional control is accomplished by designing with a minimum of mechanical joints.

The electronics module assemblies contain most of the intraconnects within themselves thus reducing interconnection problems. Flat assemblies were chosen since three dimensional modules tend to bury head producing components and place components into positions where removal for repair is impractical.

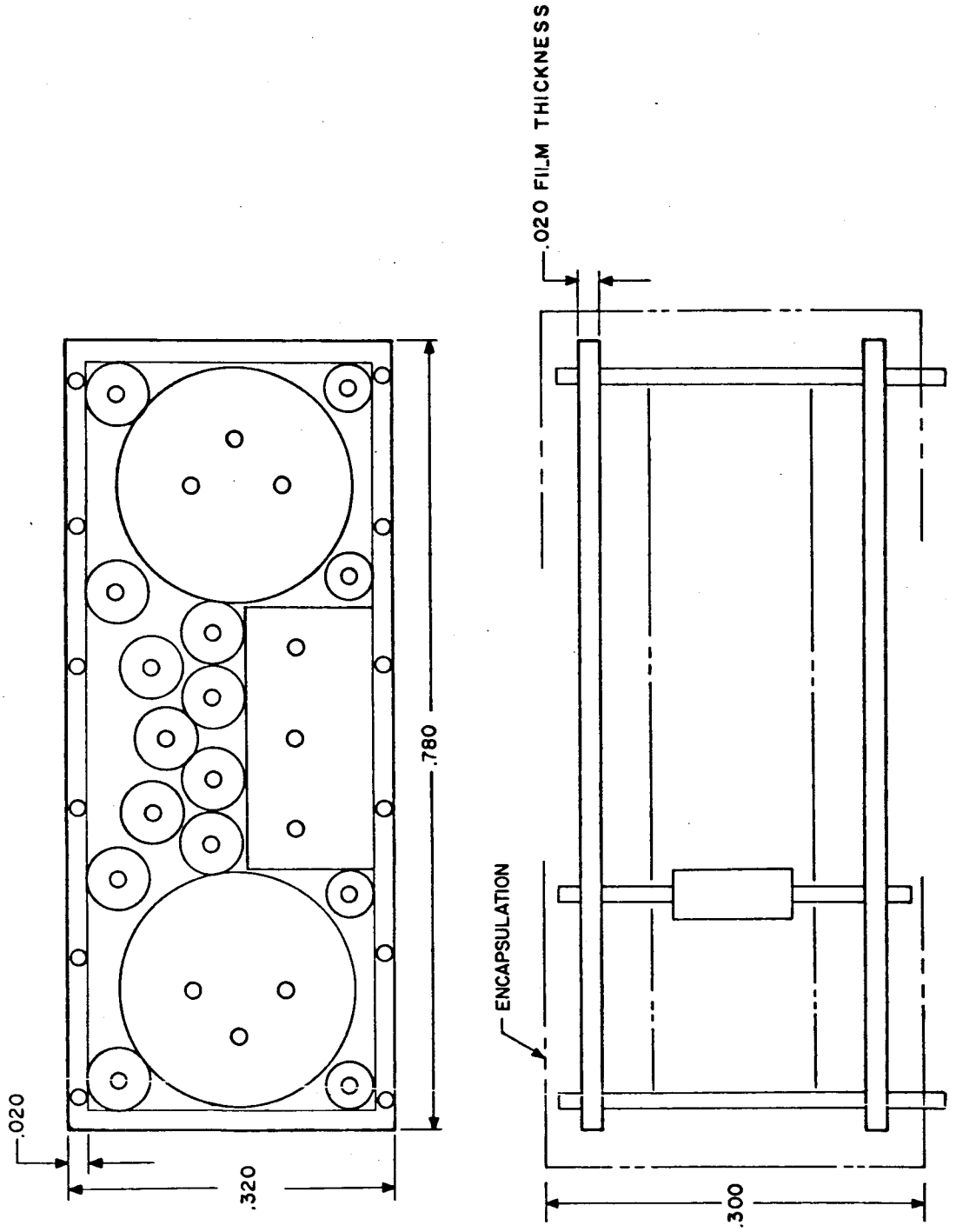


Figure 5.3-1 'D' Switch Cordwood Module Envelope Detail

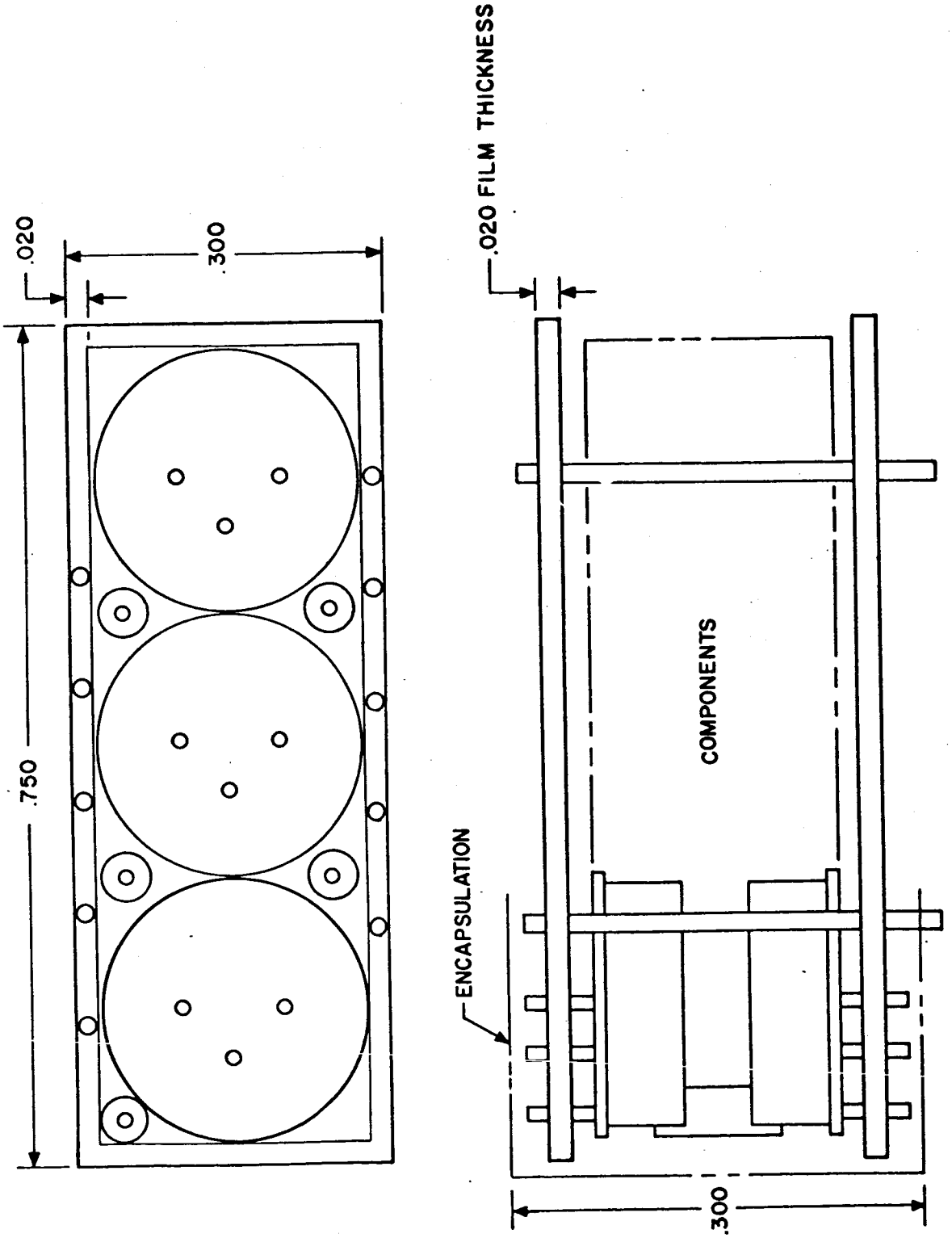


Figure 5.3-2 Marker Output Cordwood Module Envelope Detail

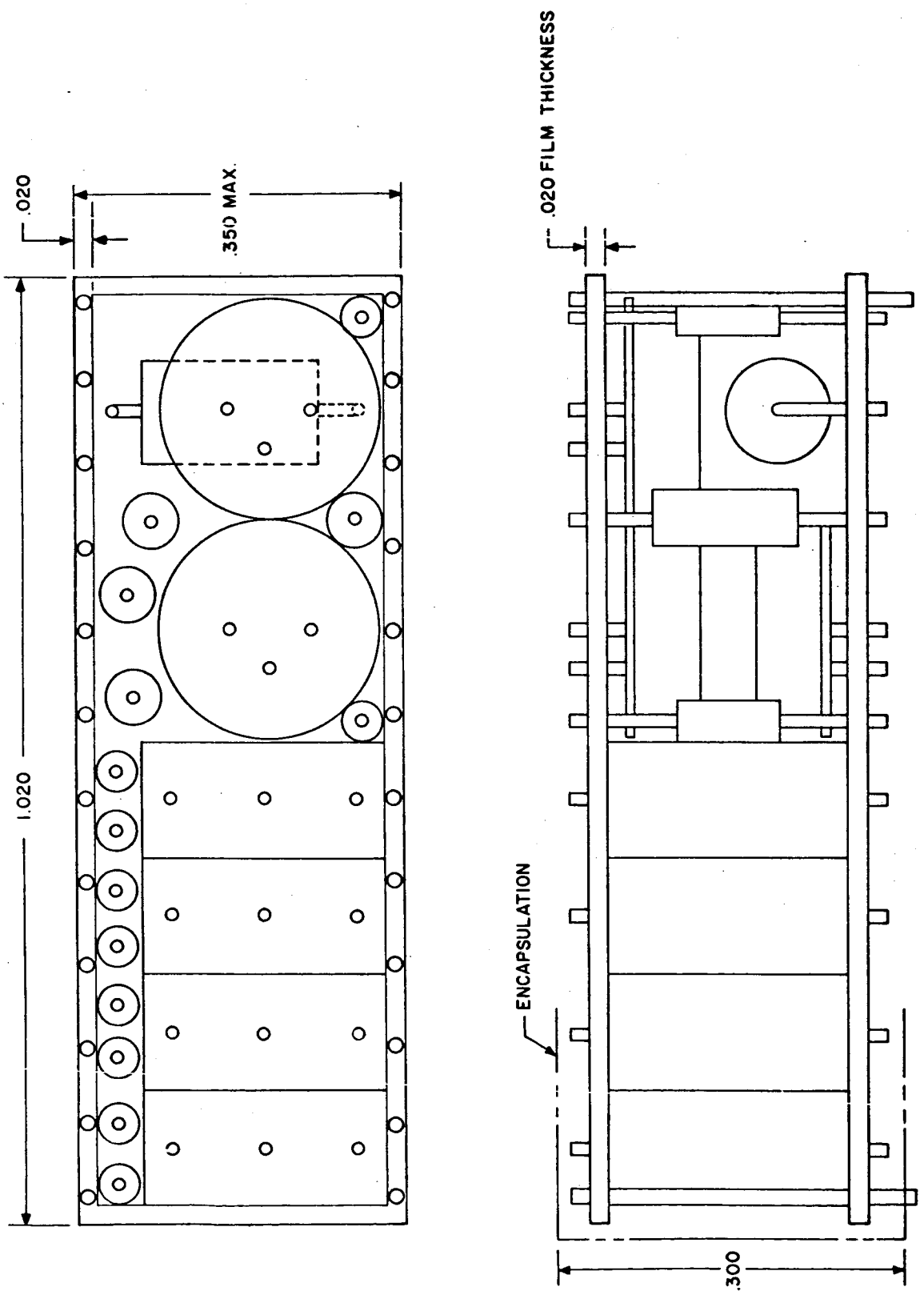


Figure 5.3-3 Bit Counter/XFMR Cordwood Module Envelope

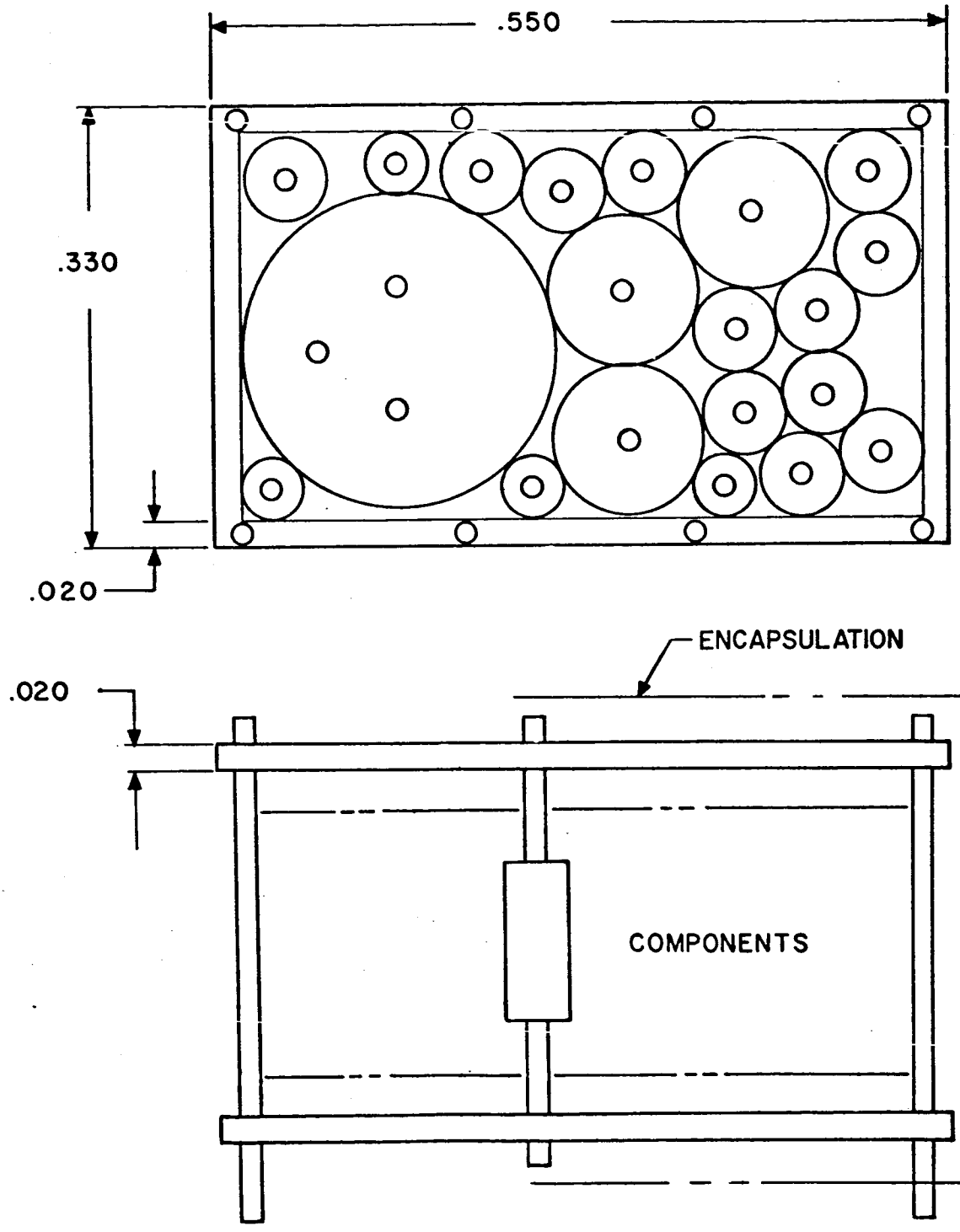


Figure 5.3-4 Bit Counter Control Cordwood Module Envelope Detail

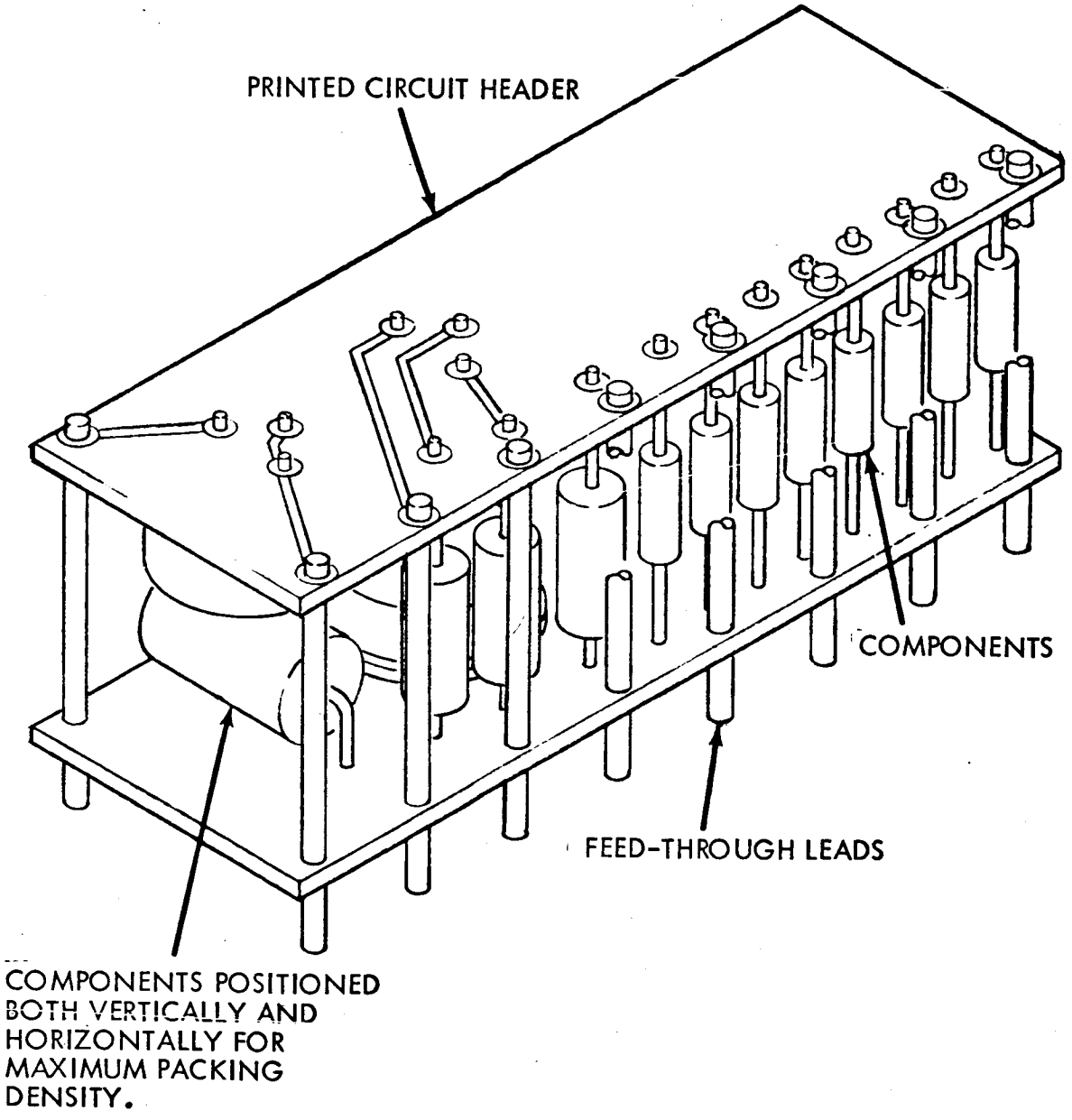


Figure 5.3-5 Typical Cordwood Module

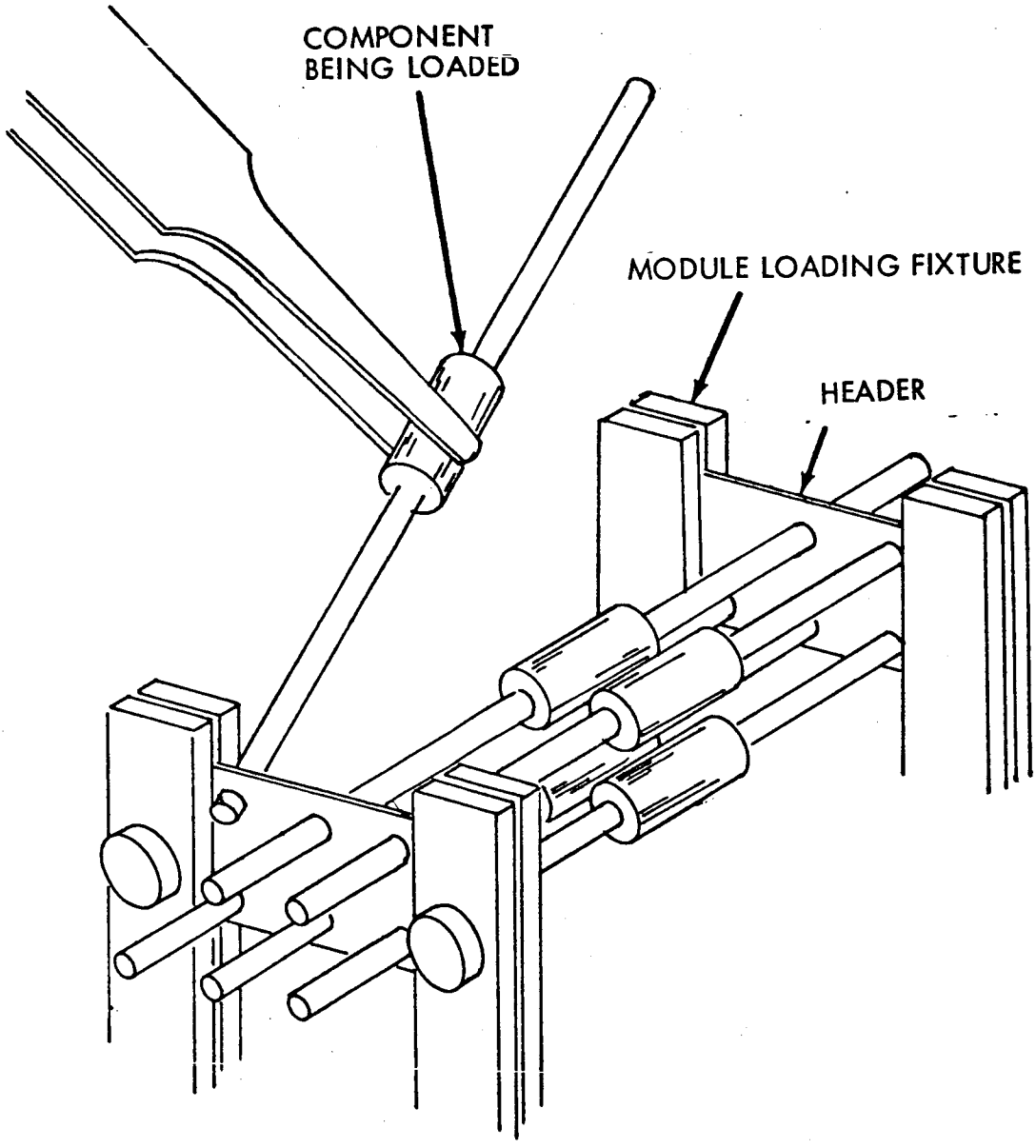


Figure 5.3-6 Cordwood Module Assembly Techniques

Printed circuitry terminates with provisions for lap soldering (re-flow) the tabs from the flexible cables. Where friction connectors are required, P. C. board tabs will be rhodium plated. Design and fabrication of the printed circuit matrix board is controlled by the Librascope specification, L180000587, copies of which will be supplied upon request.

5.3.1 Cordwood Modules

The prototype memory, as originally proposed, used monolithic and hybrid integrated circuits for most electronic circuitry in order to hold volume and weight to a minimum. Maximum utilization of commercially-available monolithic integrated circuits is still planned, but hybrids, which were to have been designed to the special needs of this project, have been abandoned in favor of compact circuit modules assembled from conventional discrete components. The following arguments bear on this matter:

1. The market volume for hybrid circuits has not developed to the point where quality controls, yields, reliability data, etc. lead to as high a degree of confidence in them as that enjoyed by discrete components, monolithic IC's, and conventional assemblies utilizing the latter components.

2. While discrete circuit modules have considerably more volume and weight than hybrid modules, the increase in volume and weight of the overall memory package is modest because space for memory stack, interconnections, and housing is not changed.

3. The tiny discrete components used in hybrid circuits are low-volume specials which are not readily available, have little reliability history, and are difficult to handle and test.

4. Tooling costs for the hybrids, while modest compared with tooling costs for special monolithic IC's, are higher than those for more conventional packaging methods.

Use of cordwood assemblies, as an approach to miniaturization and higher reliability is currently standard throughout the armed services and industry. This technique provides for increased maintainability based on the "throw-away-module" concept. Rather than component servicing, maintenance is carried to the next level where complete circuit functions are replaced with minimum down-time by semi-skilled technicians, both of which greatly reduce maintenance costs. Each cordwood module provides a complete electrical function, and may be independently tested for performance of this function. Module circuits are normally repeated segments of the overall circuit. In digital systems, they would be flip-flops, gates, inverters, etc., and in analog circuits any recognizable repeated portion of the overall circuit.

After the general appearance of the equipment was determined, and the mounting arrangement and heat conducting paths were planned, the modules were designed to the available space envelope. Where possible, all components were chosen for minimum size and uniformity in body length (extra long components may be laid crosswise to cut down volume, if necessary). The heat-generating components are separated from heat-sensitive components and placed near one of the module surfaces to allow proper heat sinking.

In welded modules, the end cards (plastic film) are used to locate, hold components in place, and provide for connection information. They are photo-reduced from the final general assembly, component lead holes are punched in the end cards and connections are made against the cards to the component leads. After assembly, joining, and embedding, the end cards remain as a part of the module. For soldered modules, printed circuit boards are used as the end cards.

Holding jigs similar to those shown in figure 5.3-6 are used to retain the end cards during assembly, while the components are wired into place. After all the circuit elements are properly positioned the end cards are moved into the final assembly position and the interconnections are made.

No component leads will be used for installing cordwood modules to the matrix. All cordwood modules will be potted with an approved epoxy compound. When required, transfer of excessive heat from a cordwood module will be accomplished from the top of the module (the side away from the matrix), thus placing the contact interface directly to the aluminum casting for heat transfer to the external package. The cordwood modules are to be a throw-away sub-circuit.

In order to achieve maximum service from soldered electronic modules, care will be taken in designing each soldered joint. Reliability of welded modules is dependent upon the selection of mating material and accuracy of the weld schedule for each joint. The same care will be taken in these soldered modules (see Table 5.3-1). Advanced soldering technology has reduced the problem of component destruction due to thermal shock during the soldering operation. The chemistry and metallurgy of each joint will be carefully investigated to insure that the optimum bonding and electrical conditions exist. The selection of soldering the cordwood modules over welding is based on Librascope's experience in high density soldering. Also, by accomplishing all fabrication in house the problems encountered in Quality Assurance are kept to a minimum.

5.3.2 Digit Electronics Module

The digit electronics consists of 36 cordwood modules of 9 different types, which are mounted onto a single matrix interconnect board. The component count per cordwood and number and type of cordwood on the Digital Electronics Module are tabulated in table 5.3-2. Table 5.3-3 provides descriptive nomenclature for the cordwood type symbols, and refers each type to the appropriate section in this report.

5.3.3 Word Electronics Module

The Word electronics consists of 18 cordwood modules of 3 different types which are mounted on a single matrix interconnect board. The same component and "type" breakdown referenced above applies to the Word Electronics Modules.

TABLE 5.3-1

PROCEDURE-SOLDER JOINT DESIGN

1. Sketch Joint - Butt, lap, hook, wrap, (Fig. A)
2. Process Limitations - Two solder systems with different melting points on short leads to prevent heat conduction back to weaken first joint, etc. (Fig. B)
3. Select solder - Consider galvanic corrosion, oxidation, thermal expansion, mechanical stability electrical conductivity.
4. Design joint - Mechanical stress, heat transfer, pre-tinning.
5. Specify Flux - For each joint or series of joints.
6. Precleaning Procedure
7. Flux application (if needed)
8. Soldering Method - Iron, resistance, dip,cascade or induction.
9. Temperature limits - Based on thermal capacity of Assembly.
10. Special Fixtures - For Production techniques
11. Post Cleaning - Degrease, solvent dip, ultrasonic cleaning, brushing, etc.
12. Inspection - Visual (contact angle, spreading and pulling, cold joints). Joint should be smooth, bright and well feathered.
13. Protective coating or embedding.

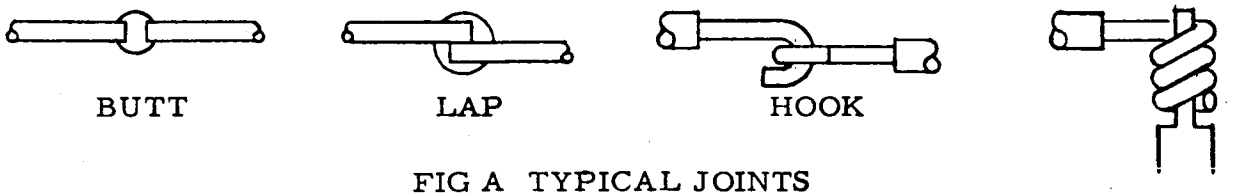


FIG A TYPICAL JOINTS

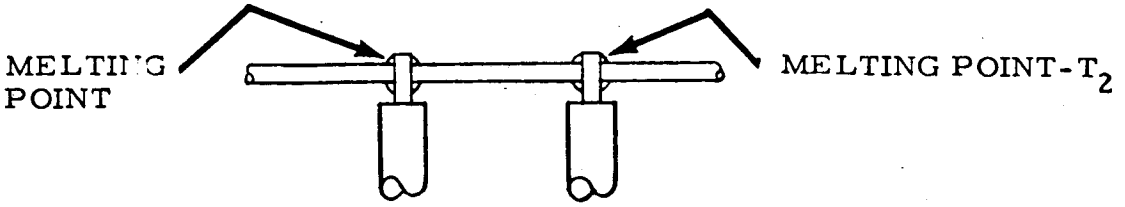


FIG B PROCESS LIMITATIONS

TABLE 5.3-2

CORDWOOD MODULES AND COMPONENT COUNT

TYPE	NUMBER CKTS	IC	TRS	TXF	DIODES	RES.	CAP.	COMPONENTS per Ckt.	COMPONENTS per Module	ESTIMATED MODULE SIZE	MODULE VOLUME	NUMBER MODULES
DIGIT ELECTRONICS MODULE												
TG	6	0	3	0	7	10	7	27	27	.55 x.50 x.3	.0825	6
BC	20	0	3	4	10	4	1	22	22	.64 x.55 x.3	.106	20
BCC	1	0	2	0	4	12	3	21	21	.46 x.39 x.3	.054	1
MO	5	0	1	0	1	0	0	2	10	.79 x.28 x.3	.066	1
DD	1	1	3	0	0	11	0	15	15	.64 x.36 x.3	.069	1
DS	4	0	4	1	6	8	0	19	19	.50 x.45 x.3	.068	4
TN	1	0	4	*See Below	3	15	5	29	29	.98 x.64 x.3	.188	1
RA	1	1	6	2	10	33	10	62		.80 x.76 x.3	.182	1
DCS	1	0	2	0	4	8	2	16	16	.45 x.40 x.3	.053	1
WORD ELECTRONICS MODULE												
WPG	1	0	3	1	1	8	2	15	15	.50 x.45 x.3	.068	1
WS	32	1/2	1	1	0	4	0	6-1/2	13	.55 x.42 x.3	.069	16
VRS	1	0	4	0	2	11	3	20	20	.51 x.48 x.3	.073	1
										ALL MODULES TOTAL	5.346	54

* (1) + (1) delay line

TABLE 5.3-3

CORDWOOD SYMBOL NOMENCLATURE

NO. MODULES IN SYSTEM	CORDWOOD MODULE SYMBOL	CIRCUITRY INCLUDED IN EACH MODULE	REFER TO REPORT SECTIONS
6	TG	One Timing Generator Circuit	3.8.1
20	BC	One Bit Register Flip and 1/20 of the Digit Selection Matrix	3.7.1 3.5.1
1	BCC	One Bit Counter Control and One Clear Signal Receiver	3.7.2 3.7.3
1	MO	Five Marker Output Circuits	3.7.4
1	DD	One Digit Driver and One Read/Write Control Circuit	3.5.3 3.8.4
4	DS	One D Switch	3.5.2
1	WPG	One Word Pulse Generator	3.6.3
16	WS	Two Word Switches	3.6.2
1	TN	One Timing Network and One Clock Receiver	3.8.2 3.8.5
1	RA	One Read Amplifier, including read transformers and shaping network	3.5.5
1	DCS	One Digit Current Sink	3.5.4
1	VRS	One Voltage-Regulator Switch	3.8.3

5.4 STACK ASSEMBLY

The memory stack assembly consists of eight woven plated wire memory mats mounted with two mats (MX-32WBO(100)D-2V5N) on each double sided printed circuit board. The memory mats contain 100 wires in the digit direction, of which 80 are plated wires, and 20 are dummy lines. Also located on the printed circuit matrix for the memory plane assemblies will be the word select diode matrix. Each word will have 2 diodes in series (as a means of increasing reliability). A total of 64 doides are used with each 32 word woven memory mat. The four (4) memory plane modules are interconnected by flexible cables (Electro-Mechanisms, Inc. or equal) and fold book-style into an assembly referred to as the memory stack. See figure 5.4-1 for memory plane layout, and figure 5.4-2 for assembled stack.

This design is highly repairable. Librascope's experience with this type of memory has shown that the only parts of the memory stack that may require replacement during assembly or for check-out are the plated wires or diodes. Repair procedures are described in Section 5.7.

The stack design was guided by the following ground rules:

1. Stress must not be placed on the plated wires by package design or assembly or their magnetic properties will be altered due to magnetostriction. This is controlled by use of a strain relief on one or both ends of the plated wire (see figure 5.4-3) for sample configurations either in use or being considered for use.

2. The capacitance between the word lines and plated wire lines must be kept as low as possible. This reduces noise coupled from word to digit lines during reading and writing. Digit line delay is also reduced. The selected encapsulant, RTV 615, has a low dielectric constant of 3.0 per ASTM D150.

3. Digit wires need to be firmly supported over their entire length. A vibration test on the bare memory fabric soldered directly to a circuit board revealed a natural frequency of 480 cps. Encapsulation of the stack is required to damp this resonant frequency.

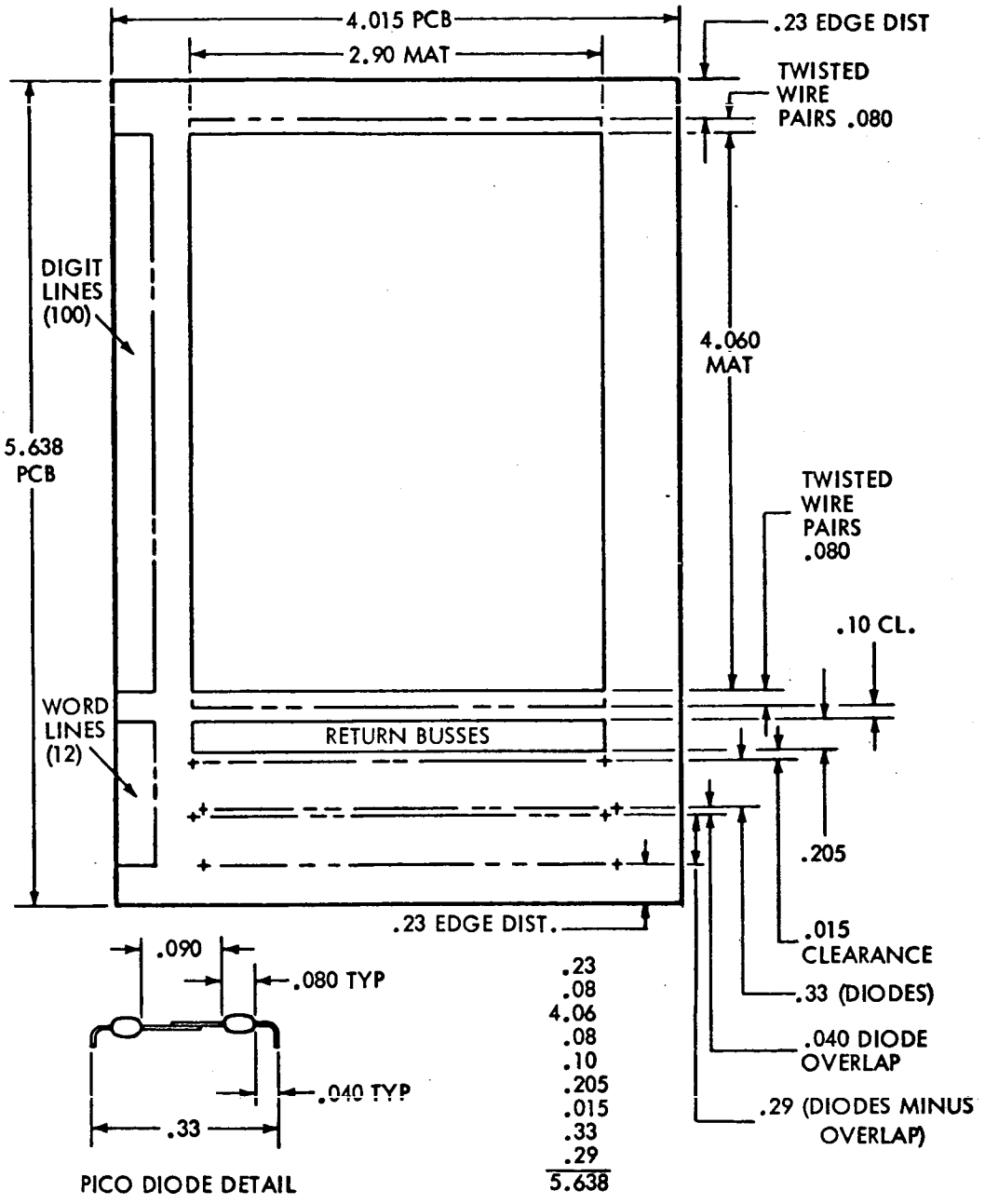


Figure 5.4-1 Memory Plane PCB Layout

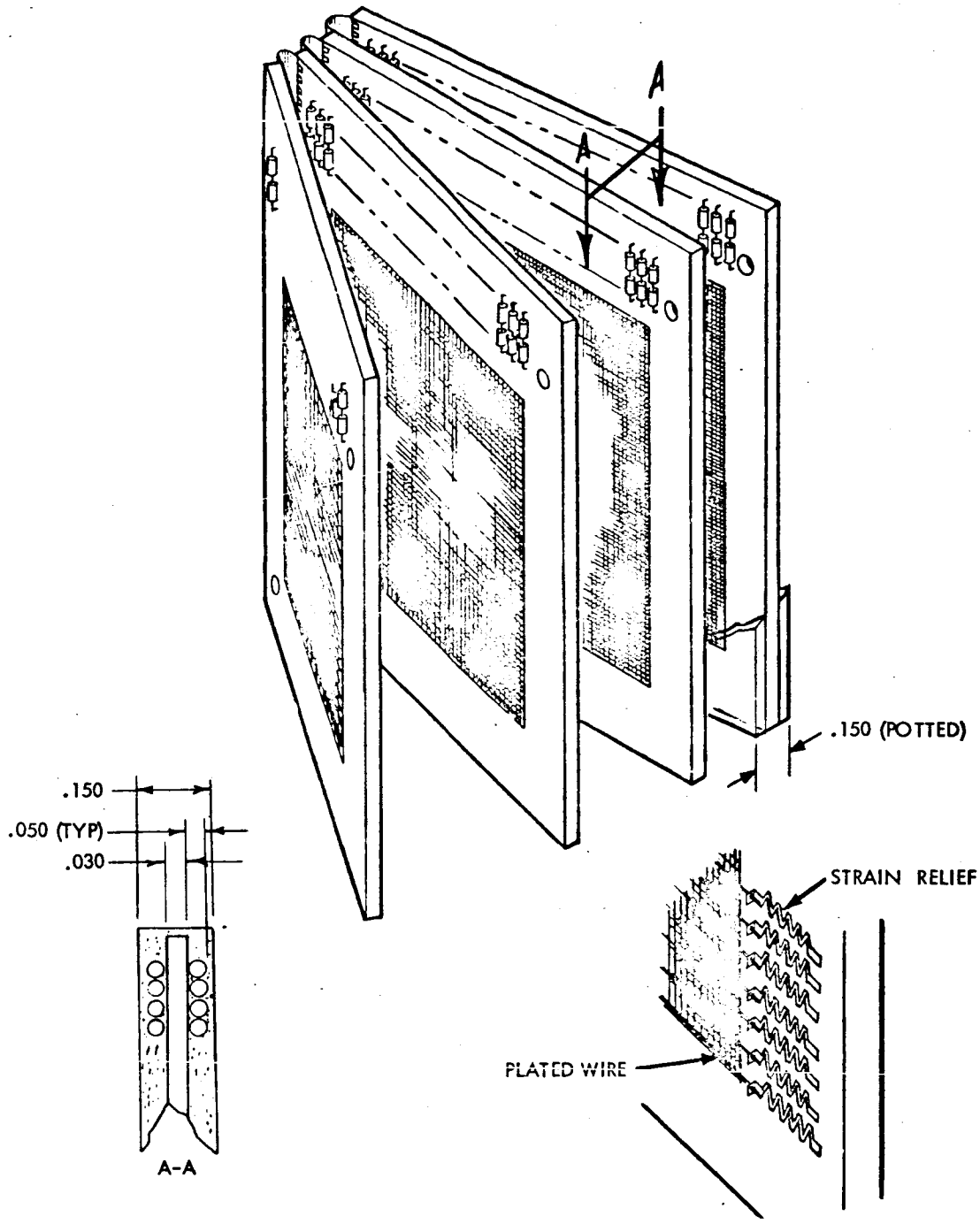
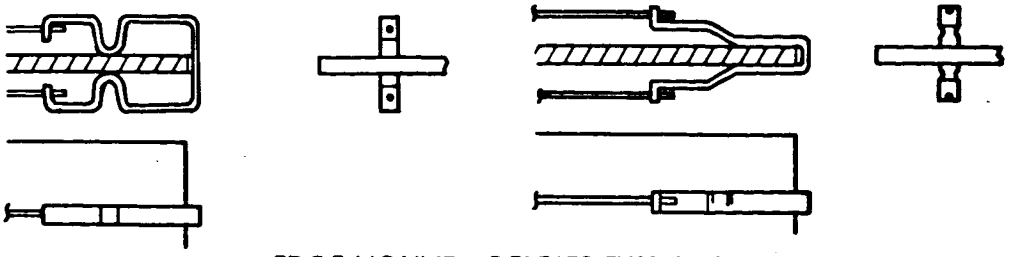
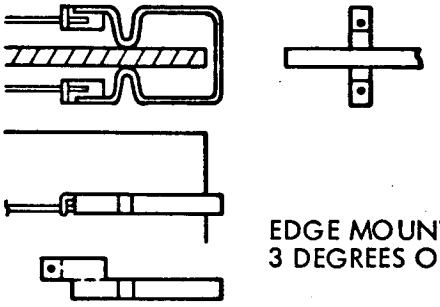


Figure 5.4-2 Memory Stack

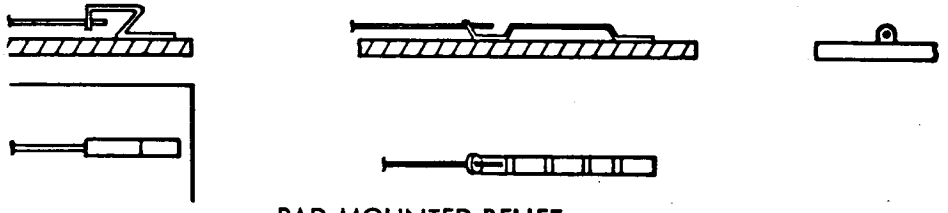
THE FOLLOWING DESIGNS OF STRAIN RELIEFS ARE UNDER CONSIDERATION FOR APPLICATIONS IN PLATED WIRE MEMORY ASSEMBLIES



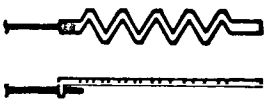
EDGE MOUNT - DELETES EXISTING PLATED-THROUGH HOLES.



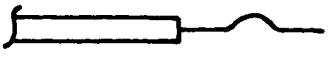
EDGE MOUNT RELIEF - 3 DEGREES OF FREEDOM



PAD MOUNTED RELIEF



PAD MOUNTED CHEM-MILLED RELIEF



MAGNET WIRE BUTT WELDED/SOLDERED TO END OF DIGIT WIRE AS STRAIN RELIEF

MAGNET WIRE WELDED/SOLDERED TO DIGIT WIRE CUT ON BIAS

Figure 5.4-3 Strain Reliefs for Digit Wires

5.4.1 Librascope Memory Module Assembly Procedure

The assembly method used for the breadboard stack (Phase I) differs somewhat from the anticipated assembly procedure to be used for the prototype (Phase II). The reason for the difference is that the prototype is to be built from mats woven at Librascope; the breadboard consisted of a repackaging of finishing Toko mats. Many of the problems encountered in Phase I will not exist in Phase II because of this difference.

The planned assembly procedure for the prototype stack is as follows:

1. The first assembly operation is to make up the terminations of the word coils. The splices are not attached to the board. They are twisted and soldered in space.
2. The word coil terminations are then insulated from each other by coating each splice with an insulating varnish (Glyptol #1276).
3. Diodes are mounted on the module circuit board to form the selection matrix. The diodes are mounted with the use of a resistance pulse soldering machine. This machine allows a precise amount of energy to be metered out to the solder connection, thereby reducing the chance of damage to the diodes. In addition the electrodes remain cool and act as a heat sink.
4. The mats are mounted on the memory module circuit board. The order in which the solder connections are made has been shown to be critical to the electrical performance of the mat. The correct sequence is:
    a. Remove dummy wires and insert plated wires in the mat where they are required.
    b. Solder the fixed end of each plated wire to the circuit board. The plated wire end must not be stressed.

c. Solder the strain relief loop to the circuit board at the floating end of the plated wire.

d. Solder the plated wire to the strain relief, again exercising extreme caution to avoid putting stresses on the plated wire.

e. The ends of the word coils are the last terminations to be made. Care shold be taken at this point to avoid distortion of the mat.

5. A complete electrical test is performed on the memory module at this time. Stresses on the plated wire that degrade electrical performance are relieved by melting the solder at both ends of the plated wire and allowing it to move to its relaxed position.

6. The memory module is embedded in a blanket of clear silicone rubber (GE #615). This material does not adhere to the mat, it merely encapsulates it. Adhesion to the circuit board is promoted by the use of a primer (GE #4155). The embedment procedure is:

   a. Prime the circuit board (mask output terminals and let it air dry for 45 minutes.

   b. Mount the assembly in the encapsulating mold and seal the mold.

   c. Mix the silicone rubber (100 parts 615A to 10 parts 615B and de-gas the material.

   d. Inject the silicone rubber into the mold slowly to avoid air entrapment.

   e. Place the mold assembly in an oven at 100°C for four hours.

   f. Open the mold carefully and trim the flash from the module.

7. At this point the circuitry is completely embedded in the potting material, except for the output pads which were masked before potting

5.5 FINAL ASSEMBLY AND HOUSING

5.5.1 Final Assembly

When the individual modules have been assembled, checked-out, and encapsulated, they are wired together to form the completed stack. The (4) memory modules are interconnected with flexible printed cable along their edges. After these connections are soldered, the bare copper of the cable and the exposed circuit board pad are potted to seal the entire assembly. The memory stack, consisting of (4) memory modules, is connected to the electronics modules in the same manner that the memroy modules are interconnected. The digit electronics module is then connected to the word electronics by a flexible cable. The final assembly is then loaded into the housing and the external interface connector(s) are mounted. The end covers are then secured in place completing the final assembly.

5.5.2 Housing

The Housing outline and installation dimensions are shown in Figure 5.2-1. A cast aluminum housing was selected over a fabricated unit for dimensional stability (particularly in wall section thickness) and cost. Elimination of mechanical joints was another determining factor when considering structural response of the system to high acceleration forces

If radiation becomes problematical, the interior of the housing can be lined with mu metal shielding. No immediate need, or advantage, is seen in encapsulating the entire memory assembly but this can be accomplished should the need arise.

This system conforms to the mounting structure specified in JPL drawing #4901045. Each part of the assembly provides structural strength to the system. The main load-carrying members of the system are the cover, the mounting frame the interconnection matrix and the stack. The system is similar to a composite beam with the modules as spacers between the elements of the beam and the silicon potting as structural dampers. This design results in a highly damped structure.

5.6 MATERIALS AND PARTS LIST

All materials proposed for use in the JPL Low Power Space Memory were selected for optimum advantages in reliability vs. size, weight, ease of handling and fabrication, availability, and cost.

Listed below are materials used in the memory stack, electronic components list, and the complete assembly parts list.

MATERIALS FOR MEMORY STACK

G-10 Epoxy Glass

Copper

Nylon

Polyurathane

GE Silicone Rubber No. 615

63-37 or 60-40 Tin/Lead Solder

Permalloy

Phosphor Bronze

Permacel P-18 Film Adhesive

G.E. Primer SS-4101

Gold

Kovar

ELECTRONIC COMPONENTS LIST

RESISTORS are Style RC05 per MIL-R-11. Where more stability is required, metal film resistors, Style RN50E, per MIL-R-10509 will be used. These are 1/20 watt resistors, same physical size as RC05.

CERAMIC CAPACITORS are U.S. CapacitorC -10 Series.

SINGLE DIODES are Microsemiconductor MC9853. Dual Diodes for the memory stack are MC9962.

TRANSFORMERS are Pulse Engineering "Flat-Tran" Series or equivalent.

ELECTRONIC COMPONENTS LIST (cont'd)

TRANSISTORS arein TO-46 Case, by special factory order.

The DELAY LINE in the TN module is Technitrol 371A800B.

PARTS LIST (MECHANICAL)

DESCRIPTION	QTY REQ'D
Low Power Memory System	--
Housing, Casting	1
Cover, Casting	2
Digit Electronics Module	1
Printed Circuit Matrix	1
Cordwood Module - Type TG	6
Cordwood Module - Type BC	20
Cordwood Module - Type BCC	1
Cordwood Module - Type MO	1
Cordwood Module - Type DD	1
Cordwood Module - Type DS	4
Cordwood Module - Type TN	1
Cordwood Module - Type RA	1
Cordwood Module - Type DCS	1
Word Electronics Module	1
Printed Circuit Matrix	1
Cordwood Module - Type WPG	1
Cordwood Module - Type WS	16
Cordwood Module - Type VRS	1
Memory Stack Module	1
Printed Circuit Matrix	4
Woven Plated Wire Memory Mat	8
Diode	512

PARTS LIST (MECHANICAL) (Cont)

	QTY REQ'D
Cable Stack-Flexible	3
Cable Digit/Word	1
Cable Input/Output	1
Cable Test Point	1
Cable Digit	1
Cable Word	1

5.7 REPAIRABILITY AND RELIABILITY

5.7.1 Repairability

The level of maintenance is the cordwood module. The modules may be replaced by unsoldering and resoldering the new unit in position. This may be accomplished with standard existing hand tools commonly found at any installation where repair of electronic equipment is done. The memory plane assembly may be replaced by removing single units containing two planes.

1. Access to the modules is accomplished simply by removing the cover from the frame assembly and lifting the module assembly out of the box. The hinging technique allows access to any module or plane assembly for inspection or repairs.

2. The cordwood modules (sub-circuits) may be replaced at any facility where simple electronic repair work is done. A soldering iron and solder sucker are the only tools required. The cordwood modules are removed by unsoldering the pins using the vacuum of the hand held solder sucker to draw away the molten solder, and then pulling the unit out of the plated-through holes. Replacements are inserted and resoldered.

3. The stack assembly repair is considerably more complex. The flexible cable is cut to release the defective plane assembly. The remaining cable on the memory stack is then stripped and the new plane assembly is lap soldered into position and bonded with an adhesive insulation tape. Repair of the plane can be carried to a lower level by replacing digit wires or diodes. To replace either component the encapsulation is cut away at the solder connections. A wire may then be withdrawn and replaced or a diode may be replaced. The encapsulation is then repaired.

5.7.2 Reliability

High Reliability is a result of the fabrication process. The high reliability of Librascope's Woven Plated Wire memories is due to characteristics inherent in the memories themselves, as well as to the fabrication process. Plating is a carefully controlled procedure. Weaving is an automatic process that eliminates many hand-assembly operations. Fabrication techniques are well known, fully proved, and themselves highly reliable. Extreme care is taken throughout fabrication, and rigid quality-control procedures are followed.

Interconnecting the sub modules to the matrix board is accomplished by soldering. This technique of assembly allows a multiple choice of bonding processes, resistance soldering, welding (series) or hand soldering. Soldering was preferred over welding throughout this program due to the repairability goals of the design.

Material selection will be made in accordance with and capable of withstanding the requirements of the JPL specifications noted and associated specifications as required.

Materials and components selected for use in the flight hardware during the packaging study will be justified with JPL, and certified to be capable of withstanding space operational environments.

This approach of hand-wiring all electrical connections except the flexible cable terminations results in higher reliability. Interconnections have been minimized by logic matrices. The word select diodes were mounted directly on the memory planes to eliminate connections to the electronics modules.

Component derating is discussed elsewhere in this report. The memory power requirements are low, within JPL specifications, thus obviating thermal stresses.

The system was designed from the start with high reliability entering every decision. To this designed-in safety is added the skilled Manufacturing and Quality Control functions developed at Librascope.

As a result of the structural analysis reported in Section 5.8, several modifications were made to the system to improve survival capability in high shock and vibration stress environments, interlocking ribs were added to stiffen the electronics modules and the aluminimum end covers. The ribs fit between the cordwood modules on the matrix. The end cover ribs are on the outside.

Four screws were added to each end cover to hold the (2) electronics modules tightly against the covers. These fasteners are in addition to the (4) studs that support the modules. This modification was incorporated due to resonance potential in the unsupported metal sections between the reinforcing ribs. These areas could act like diaphragms.

Keys were added to the housing casting that mate with slots cut in the electronics modules and the end covers. This keying will prevent any relative motion of the memory inside the housing during stress.

If hard impact landings (10,000g's) become necessary with this memory, a final precaution would be to fill all voids in the system with silicone potting compound to retard vibratory motion and damp shock pulses. This final potting could be accomplished by removing the front cover plate and filling all cavities.

5.8 ENVIRONMENTAL CONSIDERATIONS

Vibration and shock tests were performed on the breadboard memory stack. These tests are reported in Section 6. A structural analysis of the proposed prototype system was performed to calculate first order resonances. These calculations are shown in Table 5.8-1. The results of this analysis prompted the design modifications described in Section 5.7.2. Addition of stiffening sections and fasteners will damper the system to a great extent thereby raising the resonant frequencies above the levels shown in the table. However, since the problem areas had been defined and corrective steps taken, no new calculations were performed on the modified structures, except the effect of a thicker housing section, which is shown in the calculations.

The subsystem resonances shown in the table cannot be readily integrated into a composite resonant frequency for the entire system. Any such calculated composite would probably not exceed 75% accuracy and cannot predict the significant input versus output (Q) ratio. Therefore, no attempt was made to calculate the system first order resonances. This data will be obtained empirically during environmental tests of the prototype.

Table 5.8.1. Vibration and Shock Analysis

Definition of symbols used in calculations

f_m = resonant frequency (cps)

E = Young's Modules of Elasticity ($lb/in.^2$)

I = Moment of Inertia of Section (in^4)

W = Total Weight of Structure (lbs)

L = Effective Span (in.)

A = Areas of section (in^2)

P = load (lbs)

N = number of fasteners

Table 5.8.1. Vibration and Shock Analysis - Continued

K = Mode factor in vibration

μ = Coeficient of Friction

S = Coeficient of deflection of a semi-fixed beam

1. RESONANT FREQUENCY OF SYSTEM SUPPORTS (MOUNTING EARS) Consider the mounting ears of the housing to be rigidly supported and loaded at the rigid interface by the weight of the memory. (This calculation disregards attachment of the bottom of the housing to a JPL structure by two screws.) The natural frequency of the mounting ears, loaded in this manner, is as follows.

$$f_n = 3.13\sqrt{\frac{3EI}{WL^3}} = 3.13\sqrt{\frac{(3)(10)^7(0.15)^3(1.6)}{(1.77)(0.29)^3}} = 6,050 \text{ cps}$$

2. RESONANT FREQUENCY OF (4) STACK SUPPORTING STUDS Consider the (4) studs loaded with the mass of the (2) encapsulated electronics modules, (4) memory modules, cables, and under compressive loading by the tightened end covers. This equation takes into account the frictional damping of the contiguous encapsulated surfaces. The natural frequency then, of the loaded support studs considered as a semi-fixed beam is as follows. (stainless steel, shank dia. = 0.187 with end turned to No. 8-32 threads)

$$\text{(Beam Resonance) } f_{n(\text{beam})} = 3.13\sqrt{\frac{(S)EI}{(W/N)(L^3)(\mu)}}$$

$$= 3.13\sqrt{\frac{(354/2.5)(29)(10)^6(.049)(.164)^4}{(3.54/4)(1.5)^3(.55)}}$$

$$= 930 \text{ cps}$$

The axial resonance of these same studs is as follows;

$$\text{(Axial Resonance)} = f_{n(\text{axial})} = 3.13\sqrt{\frac{AE}{(P/N)(L)}} = 3.13\sqrt{\frac{\frac{(.021)(.0139)}{2}(29)(10)^6}{(3.54/4)(1.6)}}$$

$$= 1870 \text{ cps}$$

3. RESONANT FREQUENCY OF HOUSING

The natural frequency of the housing, with end covers attached, is calculated below for the (2) major axes (horizongal and vertical). These equations were written when the rear cover was an integral part of the housing. No revision has been made since the vibratory response(s) are not significantly affected by the change to a removable rear cover. Both front and rear covers are ribbed to lock with the frame.

Natural frequency of housing in horizontal plane (plane parallel to top and bottom. Wall section thickness = 0.044 inch. Equivalent distributed load per inch = 0.00851 pounds).

$$f_{n(\text{horizontal})} = 3.13\sqrt{\frac{EL^3}{KPA^4}} = 3.13\sqrt{\frac{(10)(10)^7(.062)^3}{(.085)(.0085)(1.6)^4}}$$

$$= 2220 \text{ cps}$$

Natural Frequency of Housing in vertical plane (plane parallel to front and rear covers. Same wall section thickness as above)

$$f_{n(\text{vertical})} = 3.13\sqrt{\frac{EL^3}{KPA^4}} = 3.13\sqrt{\frac{(10)(10)^7(.044)^3}{(.06)(.0085)(2)^4}}$$

$$= 1020 \text{ cps}$$

Recalculation of Housing Natural Frequency in vertical plane if wall section thickness were increased from 0.044 inch to 0.078 inch. (Equivalent distributed load per inch = 0.011 pounds.)

$$f_n(\text{vertical}) = 3.13\sqrt{\frac{EL^3}{KPA^4}} = 3.13\sqrt{\frac{(10)(10)^7(.078)^3}{(.06)(.011)(2)^4}}$$

$$= 2090 \text{ cps}$$

The above recalculation shows that the housing resonance could be moved above 2000 cycles if this (or other) contributing resonance proved to be a detrimental, dominant mode in the composite system resonance. It is not intended, at this time, to increase the wall section thickness.

5.8.1 Thermal Management

Clearly defined conduction paths with a minimum of thermal joints are mapped to transfer the excessive heat efficiently to the vehicle's structure or airframe. The most serious problem in space operation of electronic equipment, or any other heat-generating device, comes from the assembly and installation interfaces. These joints usually provide a high thermal contact resistance; this break in the heat flow path can be detrimental.

Encapsulation with silicon potting compound reduces the probability of hot spots and improves the heat transfer. Conductive cooling is the prime mode of transfer.

Installation of the final unit is accomplished through the use of four (4) studs in the cover assembly which provide a final thermal path into the vehicle structure. (Ref. JPL Dwg. D-4901045).

5.8.2 Thermal Paths

1. Thermal paths provided within the WPWM system consists of four metal studs which pass through the modules and are in direct contact (under pressure) with the external aluminum structure.
2. Each cordwood module, a potential heat source, is in direct thermal contact to the damping material bonded to the external structure.
3. The modules and their associated sub-modules have been positioned to facilitate thermal flow paths to the sides of the aluminum housing.
4. The housing then is in direct metalic contact with the vehicle at the installation interface.

NOTE: Care should be taken at the time of interfacing the WPWM system with other adjoining equipment to prohibit these equipments from using the WPWM system as a heat sink.

5.8.3 Temperature Rise

The total heat generated by the system is so low (less than 0.3 watts operating) that no thermal problems exist. The following calculations was performed to demonstrate the negligible temperature rise under worst case conditions.

Assume all heat is dissipated by conduction only, thru the system surfaces in contact with JPL structures. (Mounting ears and bottom surface).

Assume that heat is generated continuously at the maximum operating rate (0.3 watts) = 1.02 Btu/hr.

Assume the heat conductivity factor (h_c) at a conservative 40 psi clamping force against 63 rms microinches surface finish.

h_c = Conductivity factor = $\frac{500 \text{ Btu}}{(\text{hr})(\text{ft}^2)(^\circ\text{F})}$

q = Heat generated (Btu/hr)

A = Effective conductivity area

ΔT = Temperature rise

then

$$q = h_c \Delta T A$$

$$\Delta T = \frac{q}{h_c A} = \frac{1.02}{(500)\ \frac{(1.6)(6.0) + (0.6)(1.6)(2)}{144}} = 0.025^\circ\text{F}$$

This ΔT represents the thermal resistance across the interface. The absolute temperature of the system will be a function of the heat sink (structure) temperature. It may be safely assumed that the memory module will stabilize, with 1°F, at the heat sink temperature.

Section 6

EVALUATION

6.1 MEMORY EXERCISER

To evaluate the performance of the breadboard and prototype memory systems, a memory exerciser was constructed which simulates a computer or other external equipment with which the memory might interface.

Control Functions

The exerciser, illustrated in figure 6.1-1, may be controlled manually from the front panel or automatically with a digital program generator. A clock pulse must be supplied to the exerciser from a pulse generator if the digital program generator is not connected.

The manual control functions are:

1. Write in memory
2. Read from memory
3. Clear memory bit counter
4. Clear exerciser data register
5. Complement exerciser data register
6. Generate new data pattern in exerciser
7. Clear exerciser address register
8. Increment exerciser address register
9. Decrement exerciser address register
10. Selection of manual or automatic control
11. Activate comparison failure stop in automatic mode
12. Selection of breadboard or prototype memory system
13. Enter arbitrary address in exerciser address register
14. Enter arbitrary data pattern in exerciser data register.

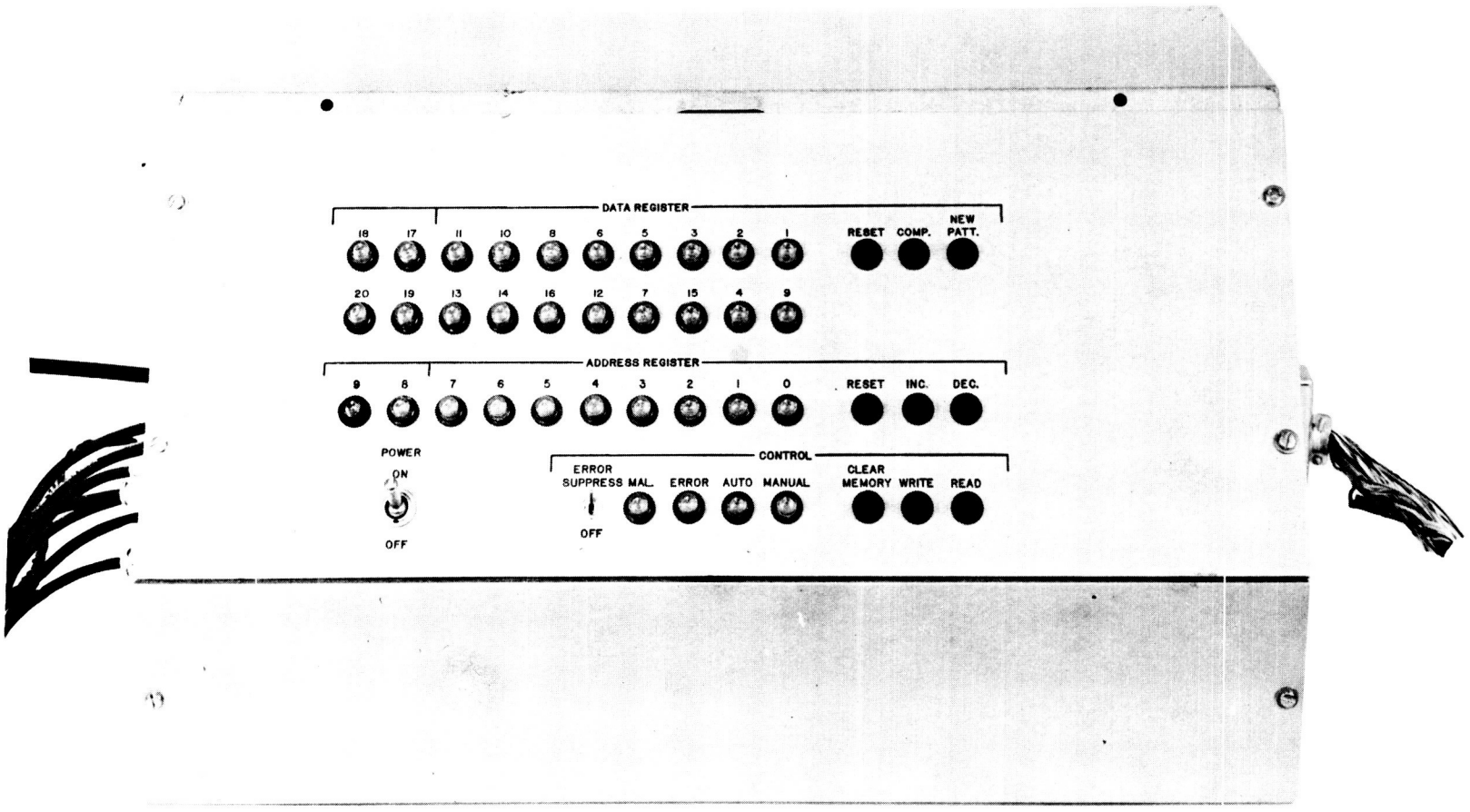


Figure 6.1-1. Memory Exerciser Front View

In addition to the above functions controlled by front panel switches, a switch behind the front panel selects the proper data register length for either the prototype or the breadboard memory.

Data is entered in the registers in the manual mode by pushing the lens caps on the register indicating lights. Corresponding flip flops are turned ON only, by switches built into the indicators.

The automatic control functions are actuated by positive pulses from a separate Digital Program Generator, such as the Computer Control Company's DPG-1. They connect into the exerciser through BNC coaxial connectors on the left side panel. They are shown in the table below.

Connector Number	Function
P1	Write in memory
P2	Read from memory
P3	Clear memory bit counter
P7	Complement exerciser data register
P5	Generate new data pattern in exerciser data register
P8	Generate new data pattern if address is all zeros only
P4	Increment exerciser address register
P6	Decrement exerciser address register
P9	Clock
-	Clear exerciser address register

The last function is implemented if Increment and Decrement inputs are given simultaneously on input connectors P4 and P6.

While in automatic mode, the exerciser can be made to stop immediately on the occurrence of an error in readout by properly setting a front panel switch.

Monitors and Indicators

Each of the address and data register flip flops has an associated neon indicator lamp on the control panel.

An error flip flop, with associated indicator lamp, will stop the exerciser if it is in "automatic" mode after execution of a read and stop command if one or more bit pairs read from memory do not compare correctly.

A malfunction flip flop, with associated indicator lamp, will stop the exerciser in "automatic" mode if the memory bit markers fail to respond when they should, or do respond when they should not.

Exerciser Organization

Please refer to the block diagram, figure 6.1-2. The data register is composed of 20 flip flops arranged into 10 randomly selected pairs. New data pattern generation is arranged so that the states of both flip flops of a pair are the same. New data pattern generation is also arranged so that the states of each pair are changed relatively frequently. Upon reading a previously written word from memory, errors may be detected by comparing the two bits of each pair.

The address register is a binary up/down counter 10 bits in length.

The exerciser has self-contained power supplies, figure 6.1-3, to make its operation independent of the memory system. The logical functions are generated with Signetics NE-Series integrated circuits.

Three timing generators required for interval timing are fabricated from discrete components. Schematics are shown in figure 6.1-4.

Connections

A power cord supplies 115 VAC 60 Hz to the exerciser power supplies.

Connections for the automatic control functions are listed above.

Power for the memory unit may be connected to P33 on the left side panel of the exerciser. A relay in the exerciser controlled by the exerciser power switch connects these inputs to power terminals in the P32 memory connector when the exerciser is ON.

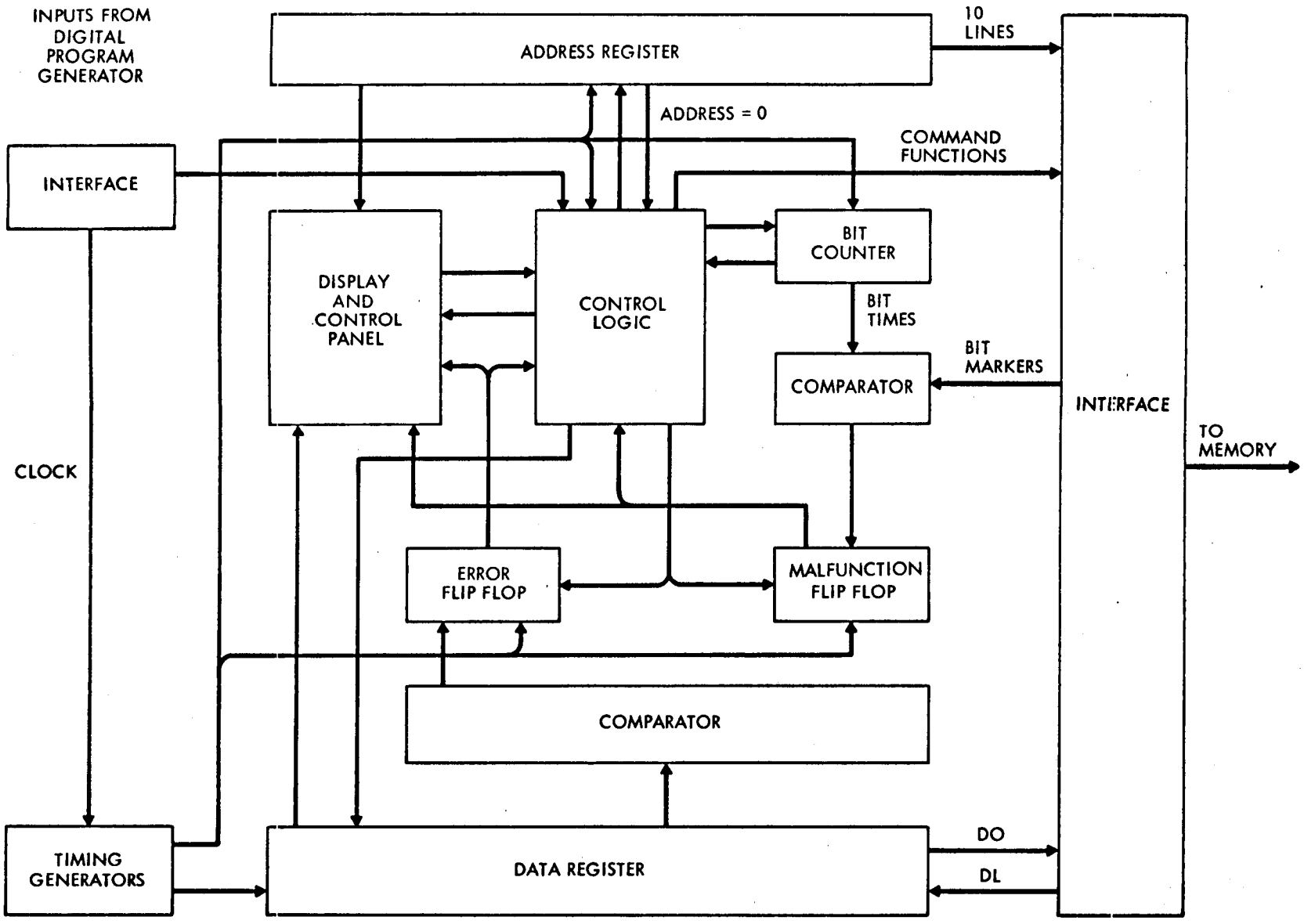


Figure 6.1-2. Memory Exerciser Block Diagram

The memory unit connects to the exerciser through Connector P32 on the right side panel. All logic signals are transmitted at standard DTL-TTL signal levels. Pin assignments are as follows:

Pin	Function
A	$\overline{A1}$ Least significant word address bit
B	A1
C	$\overline{A2}$
D	A2
E	$\overline{A3}$
F	A3
H	$\overline{A4}$
J	A4
K	$\overline{A5}$
L	A5
M	$\overline{A6}$
N	A6
P	$\overline{A7}$
R	A7
S	$\overline{A8}$
T	A8
U	$\overline{A9}$
V	A9
W	$\overline{A10}$ Most significant address bit
X	A10
Y	Data to Memory for WRITE
Z	Read/Write Control Line
a	Clock to Memory
b	Clear Signal to Memory Bit Counter
f	Bit Marker from Memory, Bit No. 1
h	Bit Marker from Memory, Bit No. 4
j	Bit Marker from Memory, Bit No. 8
k	Bit Marker from Memory, Bit No. 12
m	Bit Marker from Memory, Bit No. 16
r	Data from Memory on READ
BB	Ground
CC	-3 VDC
DD	Ground
EE	+5 VDC
FF	Ground
HH	+15 VDC

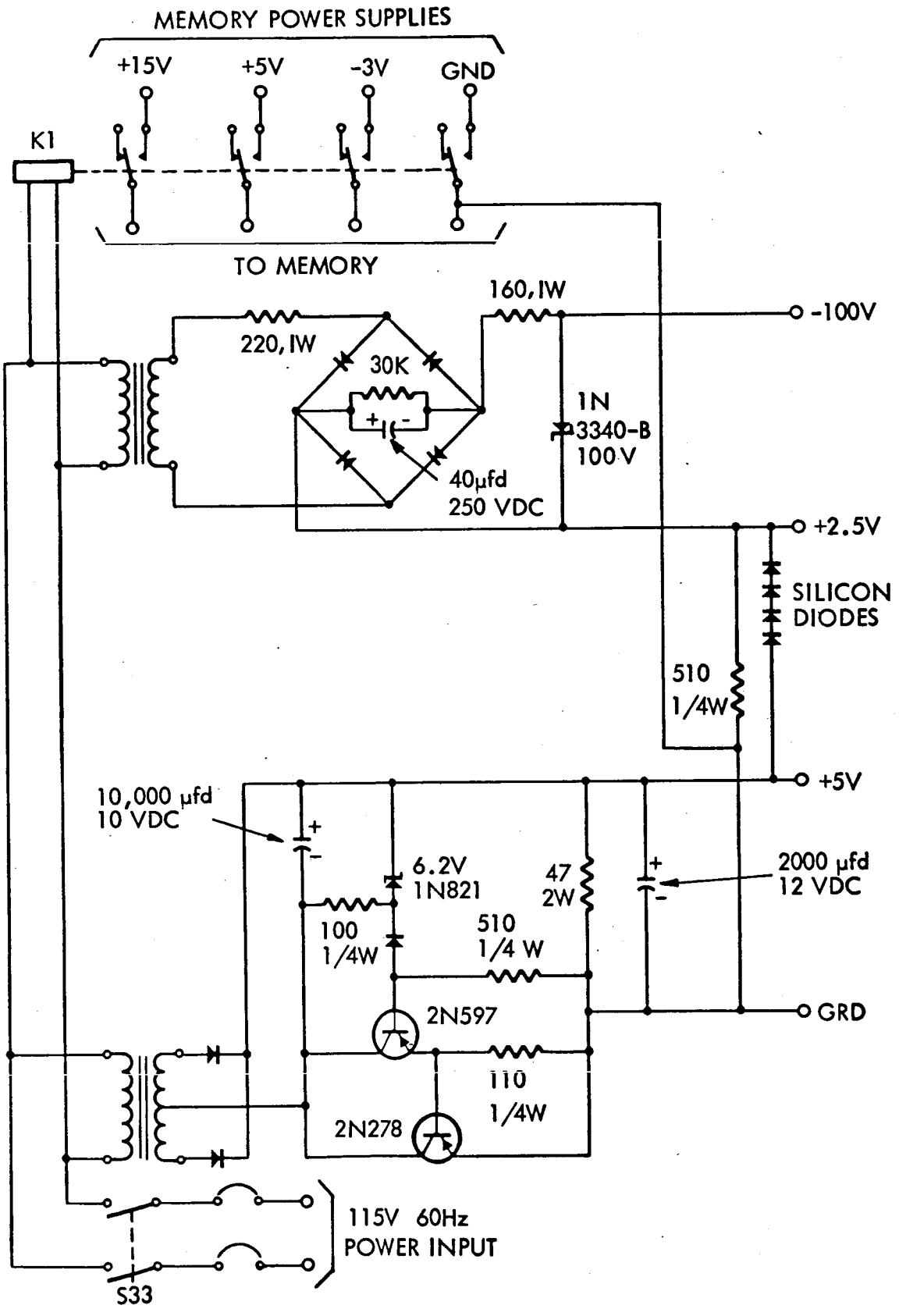


Figure 6.1-3. Memory Exerciser Power Supplies

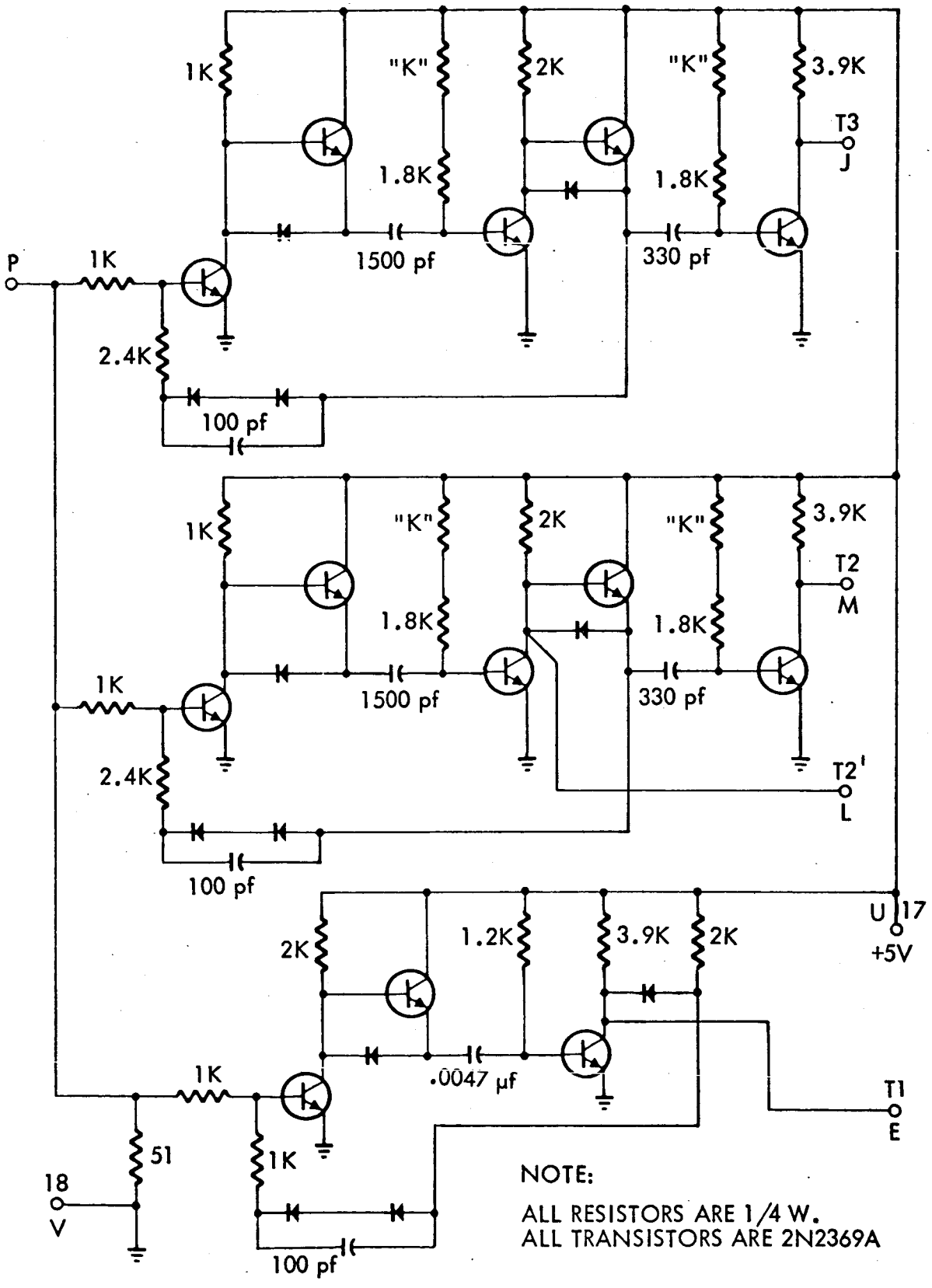


Figure 6.1-4. Memory Exerciser Timing Generator

6.2 OPERATING INSTRUCTIONS

A breadboard system layout, top view, is shown in figure 6.2-1.

Test Points

Test pins designated B1 through B16 are provided to monitor the state of each bit in the bit counter. The five marker outputs are provided with test pins marked M1, M4, M8, M12, and M16. The numbers designate the bit to which each connects.

Six test pins connected to the timing generators allow the monitoring of the timing sequence during system operation. Word current and digit current monitoring loops are provided for use with current probes. Word current flows from pin 12 to pin 13 and digit current flows from pin 6 to pin 7. Binary data output is connected to test pin DO.

External Connectors

The lines connecting the breadboard system to external equipment terminate on two connectors, JO1 and JO2. Connector JO2 provides for the address bits on eight complementary pairs of lines. Connector JO1 provides for power and input signals to the memory and feeds output data and bit markers to external equipment. Specific pin assignments are shown in the connector diagrams of figure 6.2-2.

Since the memory is designed for random addressing of words, the incoming address line pairs may be connected in random order to the addressing terminals in external equipment. However, if the pairs A1-A8 are connected to the stages of an eight-bit counter in order, least significant to most significant, then single increments or decrements of the counter will cause the memory to shift access to physically-adjacent word coils in the memory stack. This connection method is used with the memory exerciser in order to permit convenient programming of multiple disturb cycles on adjacent word lines in the stack for worst-case test patterns. Pairs A7 and A8, the most significant bits, are connected to the D switches which control digit line selection. All less significant pairs connect to word switches. Consequently, in sequential addressing, the memory steps through all word coils in the stack on a single set of 16 digit wires before changing to a

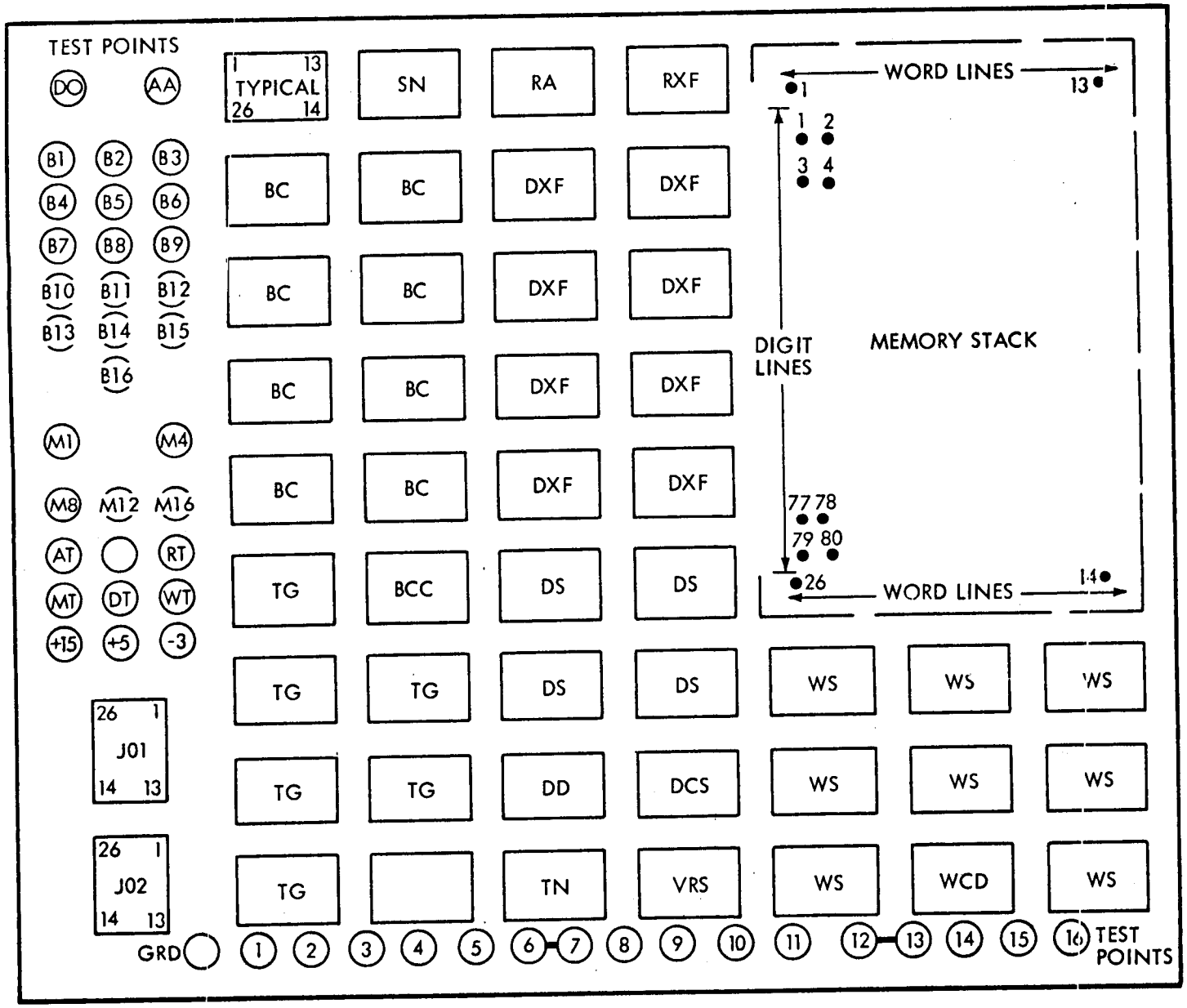
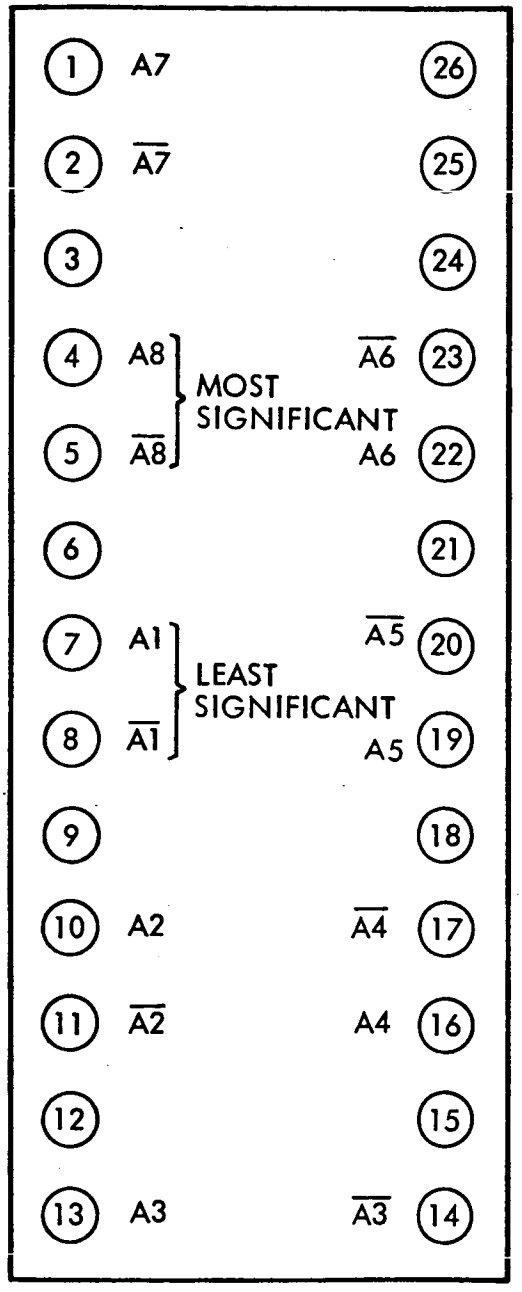
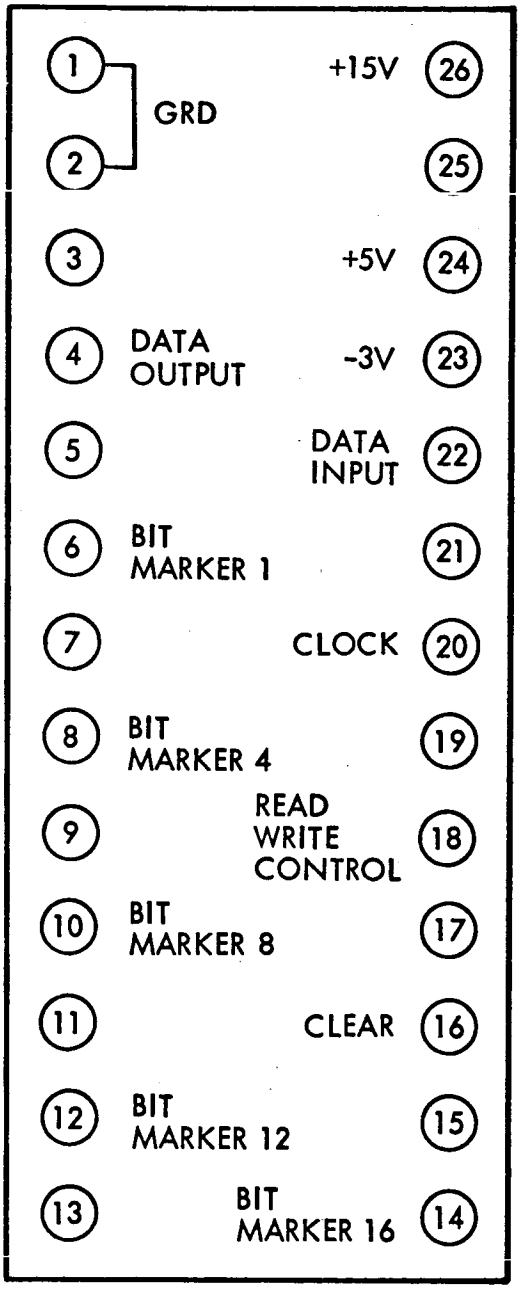


Figure 6.2-1. Breadboard Chassis Top View



J02 - ADDRESS LINES

-BOTTOM VIEW-



J01 - POWER, CONTROL, DATA, AND OUTPUT LINES

-BOTTOM VIEW-

Figure 6.2-2. Input Output Connectors

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different set. The 16 wires within the set are, of course, addressed sequentially by the memory bit counter for each externally-supplied word address.

Power Requirements

Three DC power levels must be supplied to the system. The nominal voltages are +15 Volts, +5 Volts, and -3 Volts. Tolerance on each is ±10%.

Input Signals

This section will describe the sequence of input signals to be applied to the memory system, without regard to their origin. All signals are DTL-TTL compatible. See Section 3.3 for detailed signal specifications.

1. Clear: After the application of power, a clear signal is required to set the bit counter to bit one.

2. Address: The desired word address is selected and held for 16 clock pulses while the memory accesses the 16 bits of the selected word. If desired, the address lines may be switched one microsecond after the leading edge of the clock pulse if the proper level is re-established prior to the leading edge of the next clock pulse.

3. Read-Write: The read-write control line is set for the desired operation; high for read, low for write.

4. Data: The data line is set to write 1 or 0 during a write operation only. This line has no effect on the system operation during a read cycle.

5. Clock: All signal lines listed above must be at the desired level before the arrival of clock pulses. One clock pulse is supplied to access each bit. Sixteen clock pulses will access consecutively all sixteen bits in the selected word.

Automatic Operation

For automatic operation of the memory, the following equipment is required.

1. Memory exerciser for this system (see Section 6.1).

2. Digital program generator: Computer Control Co. (now Honeywell) DPG-1 or equivalent.

3. Three power supplies.

A typical test set-up is shown in figure 6.2-3.

Connections

Connect ac power to the memory exerciser and dc power to the memory system. Connect the memory signal cables to the exerciser. Connect coaxial cables between the digital program generator (DPG) and the memory Exerciser (ME) as follows:

1. DPG Channel 1 to ME P9 (clock)
2. DPG Channel 2 to ME P1 (write)
3. DPG Channel 3 to ME P2 (read)
4. DPG Channel 4 to ME P3 (clear)
5. DPG Channel 5 to ME P4 (address increment)
6. DPG Channel 6 to ME P8 (data increment if address 0)
7. DPG Channel 7 to ME P6 (address decrement)
8. DPG Channel 8 to ME P7 (data complement)

Settings

The set-up described above is very flexible; the memory can be operated in many different patterns. The following settings are used for memory debugging and acceptance testing.

Adjust the clock output of the DPG to 100 kilohertz; adjust the step repeat channels for a repeat duration of 160 microseconds. Adjust the step pair repeat channels for a duration of greater than 170 milliseconds.

Set up program on DPG as follows:

Step	Energize Channel
1	1, 2, and 5(6)
2	1 and step repeat 2
3	1, 7, and 8
4	1
5	1, 2, and adjacent step pair repeat 5-6

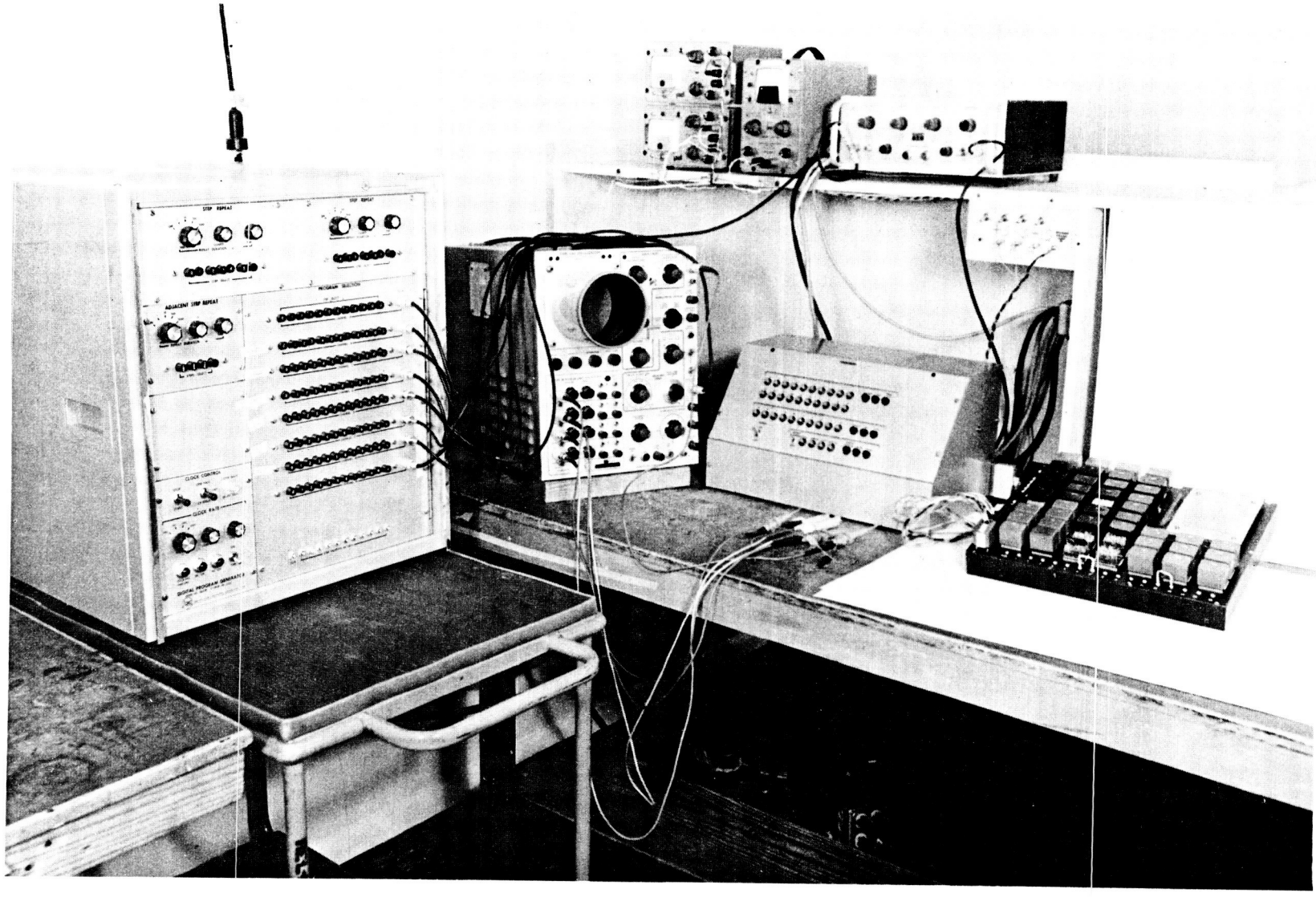

Figure 6.2-3. Typical Breadboard Memory Test Setup

Step	Energize Channel
6	1 and step repeat 6
7	1 and 5
8	1 and 5
9	1, 2, and adjacent step pair repeat 9-10
10	1 and step repeat 10
11	1 and 3
12	1
13	1 and 3, and adjacent step pair repeat 13-14
14	1 and step repeat 14
15	1
16	1

A toggle switch on the front panel adapts the memory exerciser for working with either the Breadboard or Prototype memories. This switch must be set to agree with the system under test.

Starting Procedure

Perform the following steps in order.

1. With the DPG power on and the program off, energize the memory exerciser and memory.
2. Set the memory exerciser to manual and enter the data word desired.
3. Set error suppress switch on memory exerciser at OFF.
4. Set address word to all zeros.
5. Push manual reset button.
6. Put memory exerciser into automatic operation.
7. Start DPG.

The following sequence of events will take place:

1. The address register is incremented; the data word is written into the address designated by the address register.

2. The address register is decremented and the data register is complemented.

3. The complement of the desired data word is written into an adjacent memory word at least 1,600 times.

4. The address register is twice incremented.

5. The complement of the desired data word is written into the other adjacent word in memory at least 1,600 times.

6. The address register is decremented, the data word is complemented and the original word is read at least 1,600 times. If an error is detected, the memory exerciser will switch to the manual mode and halt, displaying, in the memory exerciser data register, the word in error. The address of the word in error will be contained in the memory exerciser address register.

To restart, follow starting sequence outlined in starting procedure.

7. If the DPG is in the one-step mode, operation will halt. If the DPG is in the continuous mode, steps 1 through 6 will repeat until manually halted. For longer trials, energize Channel 6 on step 1. This will change the data word every time the program has sequenced through all memory addresses.

6.3 BREADBOARD STACK ENVIRONMENTAL EVALUATION

Two encapsulated memory stacks were fabricated for the breadboard memory stacks were fabricated for the breadboard memory system. Although the breadboard stack capacity is only one-fifth that of the prototype, the packaging design for the breadboard stacks was specifically directed toward demonstrating the design and fabrication techniques needed to produce the prototype. Environmental tests performed on the first stack included wide-range temperature, vibration, shock, dry heat sterilization and ethylene oxide sterilization. Electrical operation was tested during temperature tests, the other environmental tests were nonoperating. The second stack was tested for wide range temperature operation only.

The procedure for fabrication of the breadboard memory stacks is here reviewed briefly. Memory planes having the required electrical characteristics were purchased from TOKO, Inc. since Librascope manufacturing facilities were not in operation sufficiently early in Phase I. The purchased planes included conventional etched circuit cards and were fabricated using TOKO's standard procedures. The planes were tested electrically in Glendale before starting fabrication of the stack to establish a starting point for a continuous record of the electrical effects of the various fabrication steps. Word coil splices were then lifted from the etched circuit pads, the wires were shortened, splices were remade free of attachment to the board, and the splices were insulated. Remaining attachments to the original etched circuit card were then lifted and the entire woven mat was transferred to a new etched circuit card designed for the stack.

A second mat was installed on the other side of the new board. After soldering digit and word connections to the board and installing diodes for the word matrix, the entire assembly was encapsulated in a silicone rubber, General Electric RTV-615.

The first stack was not a success. Before any environmental tests, three word coils (out of 65) and seven digit lines (out of 80) were open or showed high resistance; all could have been repaired and some were, but in addition, a number of bits where conductor continuity was unimpaired were low in readout or could not be written to both binary states. It was subsequently determined that these troubles were caused by mechanical stresses left in the plated wires in soldering the wooven mats to the new boards. On the second stack, improved fabrication procedures were used and a thorough electrical test was made just before encapsulation; a few adjustments were made at that time. After encapsulation, all storage location were within specification limits.

Tests were performed on the first breadboard stack as follows:

1. Before starting fabrication, the two planes intended for the first stack were tested at -10°C, +25°C and +85°C. All storage locations were checked for minimum output of 2.5 mv both "0" and "1", at all temperatures. All passed. The test sequence, which includes an extensive pattern of test bit disturbs, is shown in Figure 2.4-3, and further specified in Table 2-1.

2. After fabrication was completed, the encapsulated stack was again tested electrically at all storage locations for all three temperatures for both "0" and "1". Troubles were revealed in continuity of and insulation between the word and digit coil conductors and in the magnetic properties of many storage locations, as discussed above. Some of the continuity and insulation failures were repaired. No attempt was made to relieve stresses in the plated wires which were responsible for the second class of failures. A majority of bit storage locations were still operating within specification limits and tests were continued.

3. Vibration tests were performed with the stack packaged on a structure intended to simulate its mounting configuration in the

prototype memory. Tests were performed in three mutually perpendicular directions, sweeping the range 20 to 2000 Hz, and at peak accelerations first of 1.0, then 2.5, 5.0, and finally 10.0g. Resonances were determined in each run and a five-minute frequency dwell test was run at each resonance. Maximum peak accelerations measured on the test structure at resonance were 40 and 41 in two of the three axes, and 20 g in the third. The stack was not operating during these tests. Continuity tests performed on the stack after the vibration tests showed no damage.

4. Shock tests were run on the same structure used for vibration tests. Five 200 g shocks, 2.5 msec in duration, were applied in each of three mutually perpendicular axes. Continuity tests were run after the shock tests and revealed no changes in the stack.

5. The stack was again operated in the standard test pattern, testing all bit locations for output signal level at room temperature only. No change in stack characteristics from those measured before the shock and vibration tests was observed.

6. The stack was next subjected first to the ethylene oxide decontamination procedure and then to the heat sterilization procedure specified in JPL specification VOL-50503-ETS. The RTV-615 encapsulant degreded in tensile strength and adhesion to the substrate during these tests. Reasons for the degradation are not completely clear at this time, but it is probably due to the combination of the two decontamination procedures rather than either one individually. It was concluded that the wrong primer was used on the substrate, which could account for the loss of adhesion. Discussions have been held between the manufacturer of the encapsulant, General Electric, and Librascope and JPL engineers. Furhter tests with the RTV-615 are continuing. At this time, it is

deemed likely that the problems will be resolved by changes in fabrication procedure and/or decontamination procedures; a change from the basic encapsulant is thought to be unlikely.

7. The stack was again tested comprehensively in the standard pattern at room temperature. Stresses in the plated wires and troubles in the continuity of and insulation between the word and digit conductors were still apparent. Stack characteristics were essentially unchanged from those measured before and after shock and vibration tests.

The second stack was fabricated with more detailed attention to plated wire terminations. Compehensive electrical tests at -10°C, +25°C and +85°C were run before starting stack fabrication, just before encapsulation, and afterward. During the second series of tests, mechanical adjustments were made to plated wire terminations on wires not performing to specifications. The entire stack was brough within specifications before encapsulating. Final checkout showed all bit locations to be performing within specification limits. No further environmental tests were run on the second stack.

The shock and vibration tests performed on the breadboard stack are limited in validity because the supporting structure which will interface mechanically with the stack in the flight units was not defined in time for the tests. In addition, requirements for hard impact landing now seem likely; these requirements raise the shock level to 10,000 g's. Nevertheless, it is quite conceivable that these and the other environmental tests conducted in Phase I could have indicated that the packaging design was inadequate. They did not, and the generally favorable results indicate that the present design approach should be continued and completed for the larger stack of the prototype memory unit, with modifications in encapsulating procedures as decided upon as a result of the present on-going investigations.

Detailed test reports on wide-range temperature, shock, and vibration tests are available upon request from Librascope. Results of the

sterilization tests, which were performed by JPL, are reported in JPL Inter-Office Memo 351:M778, subject "Sterilization of Memory Device," dated November 28, 1966.

6.4 SYSTEM TESTS

A fully automatic test program was set up to evaluate the performance of the memory system. The equipment used is listed in Section 6.2, Operating Instructions, and is also shown in block diagram form in figure 6.4-1.

Connections and settings were in accordance with the procedure specified for acceptance tests in Section 6.2.

System performance was evaluated at three temperature levels, -10°C, +25°C, and +85°C.

At each temperature level worst case information patterns and worst case voltage levels were used. At each temperature setting, four data patterns were examined for each memory word. In each case the procedure of Section 6.2, steps 1-7, was performed. The data patterns were:

1. All zeros.
2. All ones.
3. Zeros on all odd bits and ones on all even bits.
4. Zeros on all even bits and ones on all odd bits.

Reports on the three series of tests are as follows:

Test 1. Conditions: Temperature, -10°C
Voltage Setting, +13.5V +4.5V -2.7V
Results: Proper memory operation was observed for all data patterns

Test 2. Conditions: Temperature, +25°C
Voltage Setting, +15.0V, +5.0V, -3.0V
Results: Proper memory operation was observed for all data patterns

Test 3. Conditions: Temperature, +85°C
Voltage Setting, +16.5V +5.5V -3.3V
Results: In test pattern 2, a malfunction was observed. Stage 16 in the bit register failed to operate. The circuit module was replaced and the memory was recycled. Proper memory operation was observed.

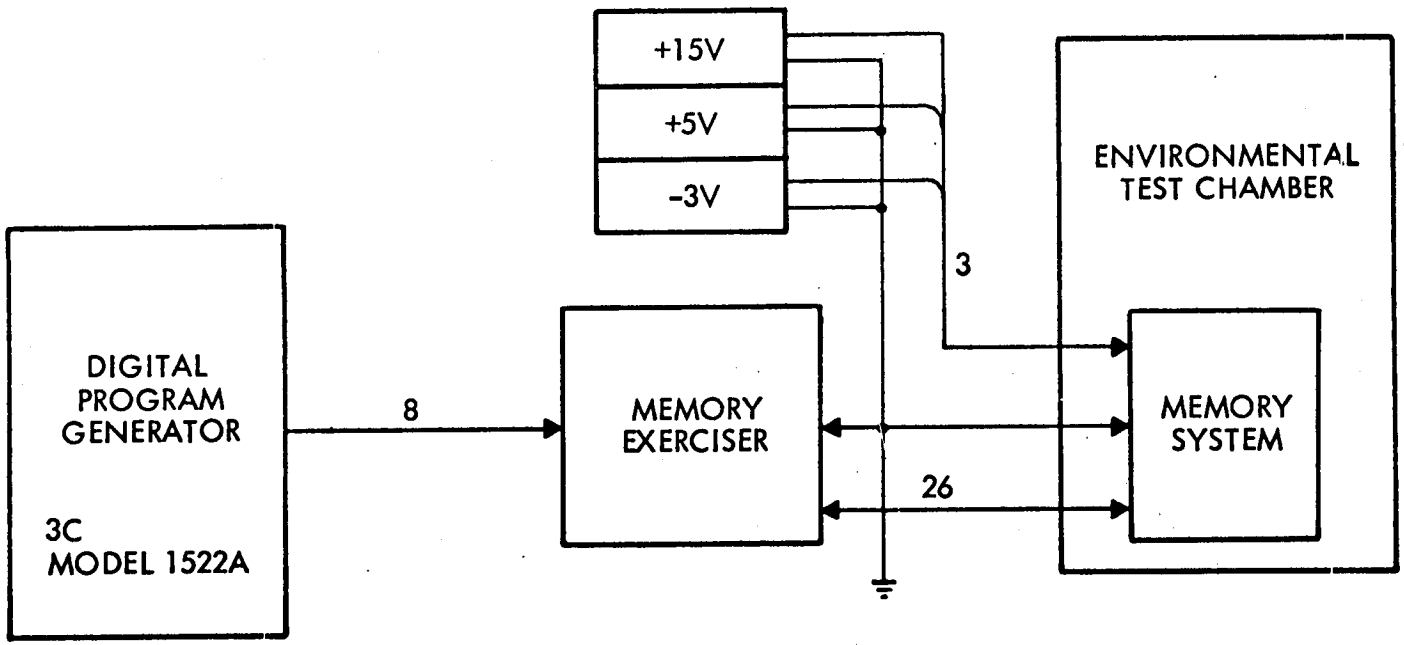

Figure 6.4-1. System Test Diagram

Oscillograph waveforms, figure 6.4-2 through figure 6.4-5, are included to demonstrate time relationships and signal patterns at key points in the system.

A radio frequency interference test was performed in the breadboard system in accordance with the test methods and procedures outlined in Jet Propoulsion Laboratory Environmental Test Specification 30236A.

Conducted interference measurements were performed on the four input power lines (+15V DC, +5V DC, -3V DC, and ground) over the frequency range of 150 kHz to 25 MHz to determine the levels of interference generated by the unit. Radiated interference measurements were performed over the frequency range of 150 kHz to 1000 MHz to determine the levels of interference radiated from the cables and the memory unit.

Conducted broadband and narrowband measurements were performed while the system was operated in "Operate Read" and "Operate Read/Write" mode. Cursory conducted and radiated tests were performed in "Standby" operation and the measured interference levels were 25 to 40 db below all other operating modes. Radiated broadband and narrowband measurements were performed during "Operate Read", "Operate Write", and "Operate Read/Write" modes.

The narrow-band conducted interference measured on all four input power leads exceeded the prescribed limits of the JPL Specification throughout the test frequency range of 150 kHz to 25 MHz during each mode of operation.

The narrowband radiated interference generated by the test sample exceeded the limits of the JPL Specification during all three modes of operation over the frequency range of 150 kHz to 25 MHz. No narrowband radiated interference was detected above 24.8 MHz during "Operate Read" and "Operate Write" modes of operation. During

"Operate Read/Write" mode of operation, the narrowband interference exceeded the specification limits from 30 kHz to 199 MHz. No narrowband signals were detected above 199 MHz.

Test results on the breadboard system are worse than those that will be encountered in the prototype because of the breadboard layout of electronic components in an open plane without shielding. Results of the present tests are not valid for the prototype. The prototype unit will be completely enclosed with a conductive shield capable of supressing radio frequency interference to below the specified level. Filters will be used on the power supply lines in the prototype to bring conducted interference levels within specifications.

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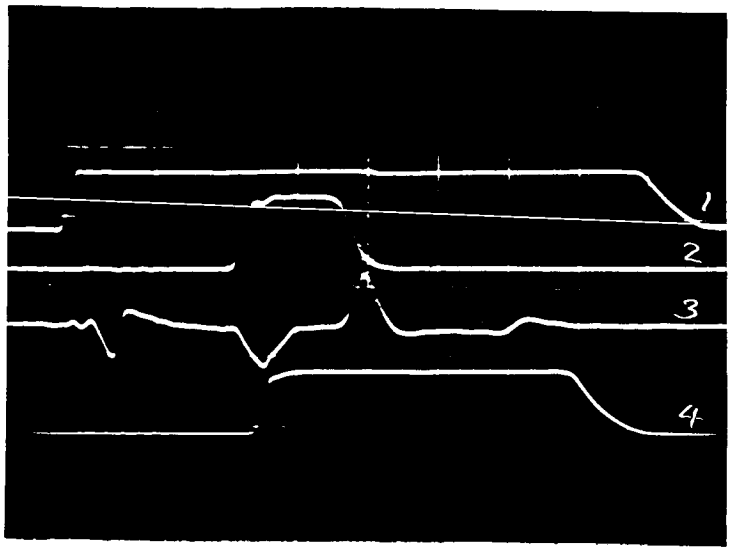
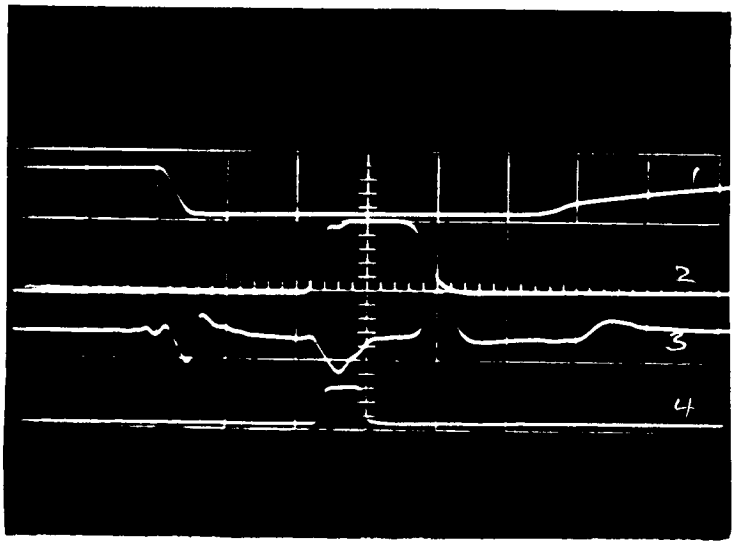


TRACE 1, MARKER OUTPUT
VERT: 5V/Cm
HORIZ: .2μSEC/Cm
TRACE 2, WORD CURRENT
VERT: 200 ma/cm
HORIZ: .2μSEC/Cm
TRACE 3, PREAMPLIFIER OUTPUT
500 mv/cm
TRACE 4, DATA OUTPUT
5V/Cm

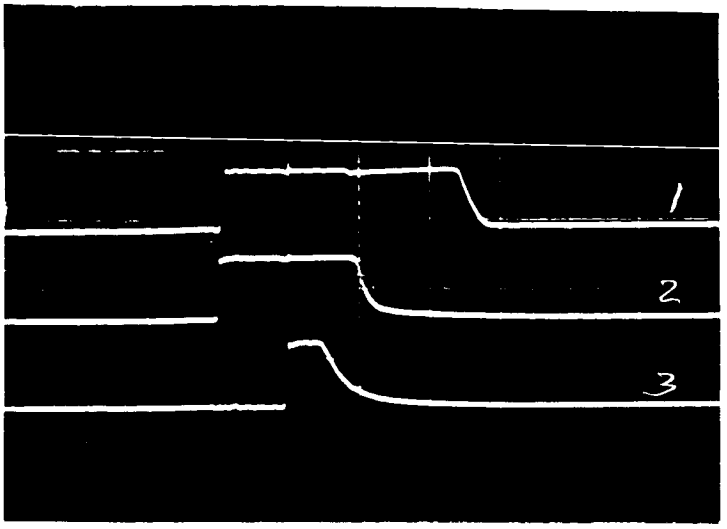
Figure 6.4-2. Marker and Data Output Relationships



TRACE 1, READ GATE
VERT: 20V/Cm
TRACE 2, WORD CURRENT
VERT: 200 ma/cm
TRACE 3, PREAMPLIFIER OUTPUT
500 mv/cm
TRACE 4, STROBE PULSE
10V/Cm

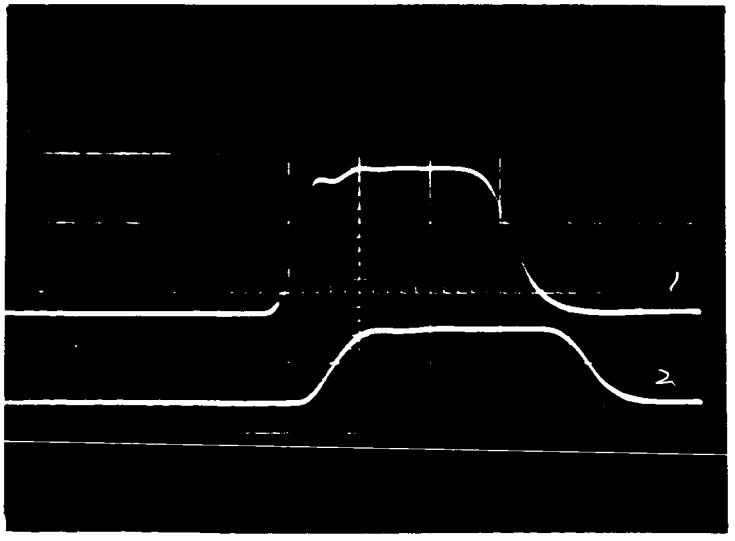
HORIZ: 200 nSEC/Cm

Figure 6.4-3. Read Gate, Signal and Strobe Relationships



TRACE 1, MARKER TIMING GENERATOR 5 V/Cm
TRACE 2, ADDRESS TIMING GENERATOR 5V/Cm
TRACE 3, DELAY TIMING GENERATOR 5V/Cm
HORIZ. 500 nSEC/Cm

Figure 6.4-4. Timing Generator Waveforms



TRACE 1, WORD CURRENT 100 ma/Cm
TRACE 2, DIGIT CURRENT 100 ma/Cm
HORIZ. 100 nSEC/Cm

Figure 6.4-5. Word and Digit Current Waveforms

Section 7

PROGRAM FOR PHASE II

Under Phase II, a prototype memory system with a capacity of 1024 words of 20 bits each will be designed and fabricated. Power consumption will be limited to 100 milliwatts standby power and 500 milliwats operating power at a read/write rate of 100,000 bits per second.

The design of the prototype will be based on the development results of Phase I, and will be in conformance with design specifications set forth in JPL Design Guidelines, dated June 11, 1965. The prototype will be tested in accordance with test procedures approved by the cognizant JPL engineer.

The completed prototype model will be packaged and delivered in flight hardware form.

It is proposed that phase II of the project be organized into six tasks:

Task II A - Prototype Circuit and System Design

Task II B - Definition of Prototype Test Procedures

Task II C - Prototype Package Design

Task II D - Prototype Fabrication

Task II E - Prototype Checkout

Task II F - Prototype Evaluation

Each of the proposed tasks is further described below.

7.1 TASK II A - PROTOTYPE CIRCUIT AND SYSTEM DESIGN

Description

Memory circuit and system designs will be modified to correct any defects noted while evaluating the breadboard or to incorporate changes in customer requirements. All circuit analyses will be critically reviewed for conformance with reliability requirements, and design modifications will be incorporated where appropriate. Modified circuits will be breadboard

and checked for performance according to circuit specifications. The breadboard memory built in Phase I will be used to check performance of modified circuits in use in a system.

Analyses of modified circuits and component selection criteria will be documented by project notebooks and will be made available to cognizant JPL personnel. Schematics and parts lists will be prepared for all circuits in a form suitable to JPL.

Duration

First through fourth months.

Output

1. Logic and circuit designs for prototype memory unit
2. Circuit schematics
3. Parts and materials lists
4. Laboratory notebooks documenting circuit analyses
5. Complete specifications for all circuits

7.2 TASK II B - DEFINITION OF PROTOTYPE TEST PROCEDURES

Description

Environmental and electrical test procedures for use on individual circuit modules and the prototype system will be devised and documented. Tests will be devised to cover the environments of operating temperature, shock and vibration, RFI, sterilization, and humidity. The environments will be those defined in JPL specifications VOL-5053-ETS, 30250B, 31252, and 30236A.

Output

1. Definition of electrical and environmental test procedures for circuit modules.
2. Definition of electrical and environmental test procedures for prototype system.
3. Written reports describing test procedures.

7.3 TASK II C - PROTOTYPE PACKAGE DESIGN

Description

Package for the prototype memory unit will be designed on the basis of the Prototype Packaging Study performed under Phase I and submitted to JPL for approval. The Phase II task will incorporate modifications to meed JPL requirements or to accommodate changes dictated by results of the breadboard evaluation. Fabrication drawings will be prepared.

Duration

First through fifth months.

Output

1. Design for the prototype package
2. Parts and materials lists for the prototype
3. Design and fabrication drawings for the prototype

7.4 TASK II D - PROTOTYPE FABRICATION

Description

The memory stack will be fabricated and encapsulated by the Librascope Memory Plane Fabrication Facility. Woven memory planes fabricated by this same facility will be used. All electronic components will be purchased from qualified outside vendors and assembled by Librascope into the prototype memory unit.

Duration

Second through sixth months.

Output

1. Woven memory planes
2. Encapsulated memory stack
3. Fabricated prototype

7.5 TASK II E - PROTOTYPE CHECKOUT

Description

The prototype memory system will be tested for compliance to room temperature electrical specifications and, if necessary, will be reworked to meet these specifications.

Duration

Seventh month.

Outputs

1. Operational prototype memory unit
2. Test results

7.6 TASK II F - PROTOTYPE EVALUATION

Description

The environmental tests defined in Task II B will be performed and reported under this task. In defining and performing these tests Librascope will be guided by JPL specifications VOL-50503-ETS, 30250B, 31252 31252, and 30236A, by all documents referenced by these specifications, and by cognizant JPL engineers.

In accordance with prior plans to use environmental specifications as design goals rather than requirements, Librascope does not intend full certification of the prototype memory unit to all electromechanical requirements for flight hardware. The time span for this program does not allow the completed prototype memory unit to be subjected to all environmental tests required for such certification. Rather, with the advice and guidance of cognizant JPL engineers, Librascope will define and perform representative environmental tests which will assure compliance to critical specifications.

All electrical specifications will be rigidly met and verified by comprehensive performance evaluation. The unit will be packaged to withstand all specified environments. The completed unit will be tested over

operating temperature extremes of -10°C to +85°C, and subjected to shock and static vibration tests as specified in JPL specification No. 30250B. Radio frequency interference tests will be performed accordinag to JPL specification No. 30236A. Compatibility with ethylene oxide decontamination and heat sterilization will be tested according to JPL specification No. VOL-50503-ETS. Compatibility with other requirements will be shown by computation rather than testing.

Duration

Eighth and ninth months.

Output

1. Performance and evaluation of environmental tests
2. Discussion of test procedures and results.